Abstract

Miniaturization is key word in microelectronics. The march towards smaller solid state electronics components has given a lot of interesting results and is now maturing into nanometre regime. This is true for both conventional CMOS technology and new emerging low dimensional structure based devices. This thesis divides its contents among some issues relevant to electrical and optoelectronic devices. The first part of the thesis is a work on nanoscaled CMOS devices and the second part contributes itself to the nanoscaled semiconductor structures.

In the first part, we have investigated four different issues related to engineering a better performance of future emerging MOS technology. The first issue deals with the cryogenic operation of ultrathin oxide MOS structures with poly-Si and Poly-$Si_{1-x}Ge_x$ gates. The main characterization tool was current-voltage (I-V) and capacitance voltage (C-V) techniques. Here, the main issue was to investigate the characteristics of flat band voltage at different temperatures and how it depends on various gate structures. We have also investigated the dependence of the accumulation capacitance for poly-Si and poly-$Si_{1-x}Ge_x$ (x=0, 0.2 and 0.35) gates. The second issue was the structural roughness and interfacial strain properties of Si/SiO_2/poly-$Si_{1-x}Ge_x$ (x=0, 0.2 and 0.35). We have employed Transmission Electron Microscope (TEM) in both image form and convergent beam electron diffraction and High Resolution X-ray Diffraction (HR-XRD) rocking curves (HR-RC) and reciprocal space mapping (2D-RSM). We found that the Ge fraction in the gate material defines the grain size and this in turn determines the strain along the Si/SiO_2 lower interface. This is in fact an interesting result, since the release or introduction of strain at lower interface (conducting channel) determines defects which consequently affect the transport properties of the channel (mobility). The third part in this section deals with qualitative assessment of oxynitridation using ion implantation as nitrogen source in a poly-$Si_{1-x}Ge_x$ gate. A time temperature study was undertaken to determine the process of nitrogen diffusion in to the silicon dioxide region. The oxynitridation takes place in the interface or in the SiO_2 region. It was found that a uniform nitrogen distribution takes place at a proper thermal processing. Finally, the overgrowth of tensile strain $Si_{1-x}Ge_x$ on fully relaxed Ge/Si (001) in uninterrupted growth sequence was investigated using HR-XRD.

In the second section of the thesis, passivation and thermal processing of nanoscaled semiconductor structures is discussed. The first paper in this section shows that hydrogen can passivate dopants in a delta doped $CdZn_{1-x}Te_x$ quantum well structures. The next paper investigates passivation of non-radiative centres like defects (dislocations) in an InAs quantum dot structure. It is shown that defect passivation can increase the radiative centres and this in turn can increase the luminescence efficiency of InAs quantum dots. The third paper gives a systematic study on the effect of thermal processing on $ZnSe_{1-x}Te_x$ ($x<0.01\%$) epilayers. It is shown that $ZnSe_{1-x}Te_x$ epilayer under proper post growth thermal annealing can give room temperature emission at a wavelength range in the visible region of 5500-7000 Å. Hydrogen passivation study done on these samples confirms the previous reports that the broad band emission is related to isoelectronic defect, i.e., excitons bound to the Te clusters. For all the above papers, we have employed photoluminescence (PL) and high resolution X-ray diffraction (HR-XRD) technique for investigation. In the last paper, we have investigated CdZnTe quantum wells for their thermal stability and HR-XRD was used for their investigation.