ABSTRACT

This thesis concerns structural and electrical characterization $Si/Si_{1-x}Ge_x$ heterostructures that are of interest for future high speed CMOS technology devices. Different complementary analytical tools were used to provide structural information.

The papers included can be divided into three main parts. First is the investigation of heterostructures which is relaxed to Ge buffer layers. Samples were grown in a chemical vapour deposition reactor (CVD). It was observed that the crystalline quality is improving a lot with a Ge layer thickness of up to 1.5μm and that the growth temperature is influencing the crystalline quality. We have also investigated the relaxation properties of a tri-layer consisting of tensile strained $Si_{1-x}Ge_x$ grown over a fully relaxed 1.5 μm thick layer of Ge on Si (001).

The second part of the thesis deals with investigating engineered MOS structures for future CMOS devices. Investigation of the microstructure and local interface strain in the poly-$Si_{1-x}Ge_x/SiO_2/Si$ tri-layer system with ultrathin oxides was performed. The result shows that for the adopted growth process, the poly grain size depends very strongly on the Ge concentration, and it increases with increasing Ge mole fraction. In addition, the presence of defects at the SiO_2/Si interface was found to be greater for samples with no local interface strain. Effect of temperature and time treatment on the distribution of ion-implanted nitrogen in poly $Si_{0.65}/Ge_{0.35}$ gate MOS samples was also studied. An optimum temperature/time cycle was achieved. Low temperature electrical characterization of ultra thin oxide MOS capacitors with p_+poly-Si_{1-x}/Ge_x and poly-Si gate was investigated. The aim of this study is to compare the low temperature performance of poly-$Si_{1-x}Ge_x$ and poly-Si gate MOS structures. Apart from the significant change in the flat band voltage, the result shows that the accumulation capacitance of these MOS structures decreases with temperature.

The third part concerns the thermal stability of different designs of $Si/Si_{1-x}Ge_x$ quantum well (QW) structures grown by CVD. To investigate the stability of the QW designs, and correlate the structural as well as the optical properties with the interlayer diffusion of these structures, we have subjected the different QWs to post-processing different temperature-time cycles. The main finding of this study is that the post growth thermal stability of this CVD grown QW is different from MBE grown samples. In addition, the design of the QW being single or double QW structure is clearly observed to affect the interlayer diffusion.