Thesis for the Degree of Doctor of Philosophy

Carbon Nanotube Transistors: Nanotube Growth, Contact Properties and Novel Devices

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COVER: Top right: Atomic force microscopy image of a carbon nanotube embedded in a trench created during electric field directed growth. Left: transfer characteristics of a carbon nanotube gated nanotube transistor sweeping both back and nanotube gates. Bottom right: Illustration of the thermionic emission over and tunneling through the Schottky barrier in a Pd-nanotube contact.

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Abstract

Carbon nanotubes (CNTs) are envisioned to be used as the basic building blocks in future electronics due to their excellent electronic properties such as high mobility, compatibility with high-k dielectrics and small diameters resulting in advantageous electrostatics. This thesis is divided into three separate topics related to increasing the fabrication yield and performance of CNT field effect transistors (CNTFETs).

The first part describes a method to control the orientation of CNTs during chemical vapour deposition (CVD) using an electric field. Under certain experimental conditions, deformations in the SiO_2 substrate are formed in the vicinity of the CNTs. An explanation based on field emission from the growing CNTs and Marangoni convection and capillary waves in the molten SiO_2 underneath agrees well with the observed structural changes.

In the second part, CNTFETs that employ CNTs as gate electrodes are described. Devices have been fabricated both by combining electric field directed growth with dielectrophoretic deposition and by a technique with two successive CVD steps. The use of a CNT gate gives an improved inverse subthreshold slope compared to using a back gate and a gate delay of 5 ps. The measured characteristics agree well with theoretical modeling which also asserts that the gate delay can be lowered to 2 ps by reducing the thickness of the gate dielectric.

The final part describes a study of the Schottky barriers between Pd contacts and semiconducting CNTs measured using temperature dependent electrical characterisation. It is found that the barrier heights are close to those expected without Fermi level pinning and inversely proportional to CNT diameter.

Keywords: Carbon nanotube, chemical vapour deposition, field effect transistor, Marangoni convection, Schottky barrier.

Appended Papers

This thesis is partly based on the work described in the following papers:

I. S. Dittmer, J. Svensson and E. E. B. Campbell.
Electric field aligned growth of single-walled carbon nanotubes
Current Applied Physics, ***4****, 595-598 (2004)*

II. J. Svensson, N. M. Bulgakova, O. A. Nerushev and E. E. B. Campbell.
Marangoni effect in SiO_2 during field-directed chemical vapor deposition growth of carbon nanotubes
Physical Review B, ***73****, 205413 (2006)*

III. J. Svensson, N. M. Bulgakova, O. A. Nerushev and E. E. B. Campbell.
Field emission induced deformations in SiO_2 during CVD growth of carbon nanotubes
Physica Status Solidi (b), ***243****, (13), 3524-3527 (2006)*

IV. D. S. Lee, J. Svensson, S. W. Lee, Y. W. Park and E. E. B. Campbell.
Fabrication of Crossed Junctions of Semiconducting and Metallic Carbon Nanotubes: A CNT-Gated CNT-FET
Journal of Nanoscience and Nanotechnology, ***6****, (5), 1325-1330 (2006)*

V. J. Svensson, Yu. Tarakanov, D S. Lee, J. M. Kinaret, Y W. Park and E. E. B. Campbell.
A carbon nanotube gated carbon nanotube transistor with 5 ps gate delay
Nanotechnology, ***19****, 325201 (2008)*

VI. J. Svensson, A. A. Sourab, Yu. Tarakanov, D S. Lee, S J. Park, S J. Baek, Y W. Park and E. E. B. Campbell
The dependence of the Schottky barrier height on carbon nanotube diameter for Pd-carbon nanotube contacts
Nanotechnology, ***20****, 175204 (2009)*

The contributions of the author to the appended papers are:

Paper I. SD and I performed the experiments. SD wrote the paper.

Paper II. I performed the experiments and the analysis, NB constructed the theoretical model, I wrote the paper together with NB and EC.

Paper III. I performed the experiments and wrote the paper.

Paper IV. I fabricated the samples together with DL. DL performed the measurements. The results were analysed by me and DL. EC wrote the paper together with DL.

Paper V. I fabricated the samples, and performed the measurements. The simulations were done by YT. I wrote the paper.

Paper VI. I fabricated the samples, and performed the measurements with assitance from AS and DL. I wrote the paper.

Scientific publications from the author which are not included since they are beyond the scope of this thesis:

- A. Gromov, S. Dittmer, J. Svensson, O. A. Nerushev, S. A. Perez-Garcia, L. Licea-Jimenez, R. Rychwalski and E. E. B. Campbell.
  Covalent Amino-Functionalisation of Single-Wall Carbon Nanotubes
  Journal Materials Chemistry, ***15****, (32), 3334 - 3339 (2005)*

- N. M. Bulgakova, A. V. Bulgakov, J. Svensson and E. E. B. Campbell.
  Possible role of charge transport in enhanced carbon nanotube growth
  Applied Physics A, ***85****,(2) ,109-116 (2006)*

- M. Tarasov, J. Svensson, J. Weis, L. Kuzmin and E. Campbell.
  Bolometer Based on Carbon Nanotubes
  JETP Letters, ***84****, (5), 267-270, (2006)*

- D. S. Lee, S. J. Park, S. D. Park, Y. W. Park, M. Kemell, M. Ritala, J. Svensson, M. Jonson and E. E. B. Campbell.
  Quantum dot manipulation in a single-walled carbon nanotube using a carbon nanotube gate
  Applied Physics Letters, ***89****, 233107 (2006)*

- M. Tarasov, J. Svensson, L. Kuzmin and E. E. B. Campbell.
  Carbon nanotube bolometers
  Applied Physics Letters, ***90****, 163503 (2007)*

Contents

List of Abbreviations and Symbols

Abbreviations

AFM	atomic force microscope
ALD	atomic layer deposition
CNT	carbon nanotube
CNTFET	carbon nanotube field effect transistor
CVD	chemical vapour deposition
DEP	dielectrophoresis
DOS	density of states
EBL	electron beam lithography
FET	field effect transistor
ITRS	International technology roadmap for semiconductors
KPFM	Kelvin probe force microscopy
MOSFET	metal-oxide-semiconductor field effect transistor
MWCNT	multi walled carbon nanotube
PECVD	plasma enhanced chemical vapour deposition
SB	Schottky barrier
SEM	scanning electron microscope
SDS	sodium dodecyl sulphate
SWCNT	single walled carbon nanotube
TEM	transmission electron microscope

Symbols

A	contact area
A_d	drain contact area
A_s	source contact area
A^*	effective Richardson's constant
A_e^*	effective Richardson's constant for electrons
A_h^*	effective Richardson's constant for holes
C_{BG}	back gate capacitance
C_{CNTG}	carbon nanotube gate capacitance
C_g	gate capacitance
δ	interfacial layer distance
d	diameter of carbon nanotube
D_{it}	density of interface states
D_p	diffusion constant
e	elementary charge
E_F^{CNT}	Fermi level in carbon nanotube
E_F^{met}	Fermi level in metal
ϵ_0	permittivity of vaccum
ϵ_r	relative dielectric constant
f_m	Fermi distribution in metal
f_{CNT}	Fermi distribution in carbon nanotube
F_x	local electric field
G	conductance
h,$\hbar$	Planck's constant
I_d	drain current
I_{de}	drain electron current
I_{dh}	drain hole current
I_{on}	on state current
I_{off}	off state current
I_s	ionisation potential
I_{sat}	saturation current
I_{se}	source electron current
I_{sh}	source hole current
k_B	Boltzmann constant
L	length of carbon nanotube

μ	mobility
μ_{FE}	Field effect mobility
m^*	effective mass
n	ideality factor
(n, m)	chiral indices
p	concentration of holes per unit length
φ	electrostatic potential
Φ_0	charge neutrality level
ϕ_{CNT}	CNT work function
ϕ_m	metal work function
Φ_{SB}	Schottky barrier for either holes or electrons
Φ_{SBe}	Schottky barrier for electrons
Φ_{SBh}	Schottky barrier for holes
Q	charge on semiconducting CNT
ρ	charge density
S	inverse subthreshold slope
s	surface tension
τ	intrinsic gate delay
τ_0	scattering time
t_{di}	thickness of dielectric
T	temperature
U_b	energy at top of Schottky barrier for holes
V_{BG}	back gate voltage
V_{CNTG}	carbon nanotube gate voltage
V_d	drain voltage
V_{dd}	power supply voltage
V_g	gate voltage
v_p	drift velocity of holes
V_{th}	threshold voltage
χ	electron affinity

Chapter 1

Introduction

The modern transistor is, in spite of its simple function, one of the most sophisticated devices created by mankind. The 10^{18} transistors fabricated annually in the world play a crucial role in computers, cell phones, power relays and a variety of other electronic devices. The rapid development of integrated circuits, with a doubling of the number of transistors on a processor chip every two years, a trend known as Moore's law [1, 2], has to a large extent been enabled due to the improvement of a transistor design based on Si. By scaling down dimensions, increasing charge mobility by introducing strain in the material, using gate dielectrics with high dielectric constants and designing new gating geometries, the performance of Si transistors has been pushed close to its physical limits. An indefinite continuation of the improvement is impossible since leakage currents increase power consumption and the electrostatics of small devices that lead to short channel effects, degrade the performance as transistor dimensions are further reduced. Due to the large economic incentive in the performance improvement of computers, both industry and academia are putting a lot of effort into the research of new materials and device designs suitable to replace Si by enabling more efficient current transport properties and improved electrostatics. According to the International Technology Roadmap for Semiconductors (ITRS)[1] among the most promising materials are III-V compound semiconductors, nanowires and carbon nanotubes (CNTs) [3].

CNTs are thin hollow cylinders of carbon which are being considered as channel material in transistors (CNTFETs) due to their high charge car-

[1]The ITRS is an organisation that identifies the technological requirements of the semiconductor industry 15 years into the future.

rier mobility that exceeds most other semiconductors [4], resilience to high current densities [5], simple integration with various gate dielectrics [6] and good electrostatics due to their small diameter. A special feature of CNTs is that they can be either metallic or semiconducting just depending on their structure. Since only semiconducting CNTs are interesting as channel material in transistors, and the type can not be reliably controlled during production, the yield of functioning transistors is typically low. It is also difficult to control both the position and density of CNTs which means that each CNT has to be located and the transistors made individually. Thus, the massive parallelism of photolithography which is the foundation of the success of integrated circuits can not be fully exploited for CNTFETs yet. Another challenge is the lack of reproducibility with devices showing a large variation in important transistor parameters such as threshold voltage, on-currents and switching speed. The main reasons for the variability of device performances is the lack of control of the dimensions, doping and contact properties of CNTs. Therefore, in spite of their excellent electrical properties, large scale integration of CNTs into modern computing architectures that require billions of operational transistors on a single chip has not yet been realised.

The electronic properties of CNTs make them not only suitable for transistors but also for applications such as gas sensors [7], high frequency diodes [8], light emitting diodes [9] and efficient photovoltaic devices [10]. Due to their high strength and low density CNTs are attractive for nano-electromechanical systems (NEMS) [11], for thin conducting sheets [12] or in composite materials [13]. The high aspect ratio of CNTs is also a suitable property for tips for scanning probe microscopy [14] and field emitters for flat panel displays [15] while the large surface to volume ratio can be exploited for hydrogen storage in fuel cells [16] or capacitors [17].

Even though the large investments in CNT science and technology are motivated by the expected commercial applications there is also a profound interest in more fundamental physics. Due to their one dimensionality, CNTs exhibit exotic quantum mechanical effects such as Luttinger liquid behaviour [18], Klein tunneling [19] and Wigner crystal localisation [20]. By introducing potential barriers in the CNTs it is also possible to create zero dimensional quantum dots that can be used to study Kondo physics [21], excited states [22] and be used for quantum computation [23]. There are also hopes that the quantum limit of mechanical oscillations in a macroscopic object can be detected in vibrating CNTs [24].

The work presented in this thesis is divided into three different topics, each

related to improving the yield and performance of CNTFETs. In chapter 4 a method where an electric field is applied during growth to control the orientation of CNTs is described. Under certain experimental conditions, deformations in the SiO_2 substrate are created and an explanation of their formation based on Marangoni convection and capillary waves is discussed. In the second part in chapter 5, a novel CNTFET which has a metallic CNT acting as a gate for a semiconducting CNT is described and electrical measurements show that a fast switching is possible due to the short gate length defined by the CNT diameter. Finally, the results of a study of the Schottky barriers present at CNT-metal contacts and their dependence on CNT diameter and the contact metal work function are discussed in chapter 6. It is found that low Schottky barriers for Pd-CNT contacts can only be obtained if the CNT diameter is 2.5 nm or larger. Any chapter dealing with one of the three different topics can be read independently and prior knowledge of the content of the other two is not needed. However, a reader not familiar with CNTs and CNTFETs is strongly encouraged to start with the introduction in chapter 2. Since this is a compilation thesis where the most important research papers are attached, the results presented in the papers are repeated as little as possible in the introductory chapters. Instead the emphasis has been put on introducing the different topics, describing methods, and discussing the results. The reader is therefore encouraged to read the attached papers to get a more complete understanding of the results.

Chapter 2

Background

In this introductory chapter the structure of CNTs is explained and their unique electronic properties discussed with emphasis on the properties relevant for electronic applications. For a more in depth description of the fundamentals of CNT science there are several excellent books available [25, 26]. In addition, there is an abundance of literature for the reader who is more interested in specific applications of CNTs [27–30].

2.1 Structure of carbon nanotubes

Carbon is a versatile element which can form an abundance of various chemical compounds. The crystalline forms of carbon are limited to a few allotropes (figure 2.1) with the most abundant being diamond and graphite. The origin of the versatility of carbon is the possibility of hybridisation of the orbitals of the valence electrons. Carbon has four valence electrons, two in s orbitals and two in p orbitals. Since it is energetically favourable to maximise the number of bonds, one s electron can be excited to the empty p orbital and one, two or three of the p orbitals mix with the remaining electron in the s orbital. In diamond which has a sp^3 configuration one s and three p orbitals hybridise to give rise to four new orbitals (figure 2.1e) while in graphite which has a sp^2 configuration, only two of the p orbitals hybridise with a s orbital to give three orbitals that lie in a plane leaving the p_z orbital unaltered (figure 2.1f). The sp^3 hybridisation in diamond results in each carbon atom having four strong covalent σ bonds to its

neighbours while the sp^2 hybridisation in graphite causes each carbon atom to form three σ bonds that lie in a plane while the remaining p_z orbitals form weaker π bonds. This leads to very different mechanical and electrical properties for the two allotropes even though their constituents are identical.

While diamond and graphite have been known for a long time, other allotropes such as fullerenes (figure 2.1c) and CNTs (figure 2.1d) have been discovered fairly recently. Observations of CNTs were made as early as 1952 [31, 32] but these discoveries were not fully understood or appreciated by the scientific community. It was not until Iijima published transmission electron microscope images of CNTs and correctly proposed their structure in 1991 [33] and 1993 [34] that interest in the field started to grow.

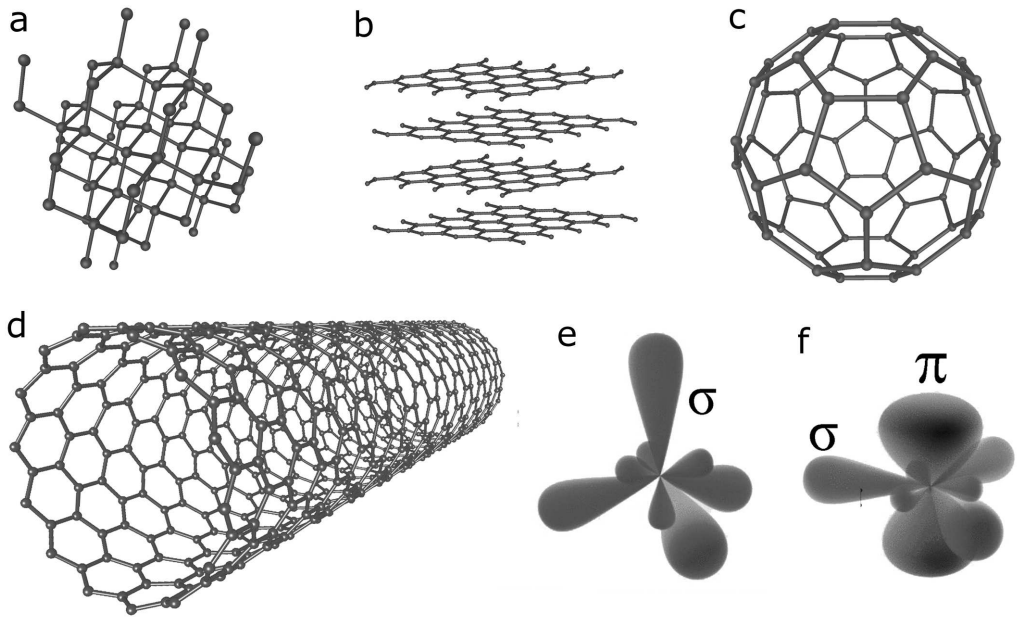

Figure 2.1: *a-d) Crystal structure of a few carbon allotropes a) Diamond b) Graphite c) C_{60} d) CNT. e) sp^3 hybridised orbitals forming σ bonds. f) sp^2 hybridised orbitals forming σ bonds and the remaining p_z orbital giving rise to π bonds.*

A single walled CNT (SWCNT) is a hollow cylinder of a hexagonal arrangement of carbon atoms which has a diameter from 0.3 nm up to a few nm and can be 10s of centimeters long [35]. There are also multiwalled CNTs with concentrically stacked shells, but while multiwalled CNTs are often used to improve the mechanical and electrical properties of composite materials

and for field emission devices, SWCNTs are more suited for transistor applications due to their smaller size and advantageous electrical properties. Therefore, the emphasis in the rest of this thesis is on SWCNTs and the abbreviation CNT refers to single walled tubes.

One way to conceptually describe the structure of a CNT is to start with a single sheet of graphite, known as graphene. A narrow strip is cut out from the sheet in a specific direction and then rolled into a seamless cylinder (figure 2.2). Depending on the direction the sheet is cut, the CNT will have a different structure affecting mainly its electronic properties. By taking the unit vectors of the hexagonal planar lattice and multiplying by the integers m and n a resulting vector $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ is obtained which defines the circumference of the CNT. m and n are called the chirality indices and uniquely determine the structure of the CNT. CNTs with indices $n = m$ are called armchair, those with $n = 0$ zigzag and the rest are referred to as chiral tubes. The diameter of a CNT can be calculated from the chirality indices by

$$d = \frac{\sqrt{3}a_{C-C}\sqrt{m^2 + mn + n^2}}{\pi} \tag{2.1}$$

where $a_{C-C} = 1.42$ Å is the nearest neighbour distance between carbon atoms [26]. It should be noted that this conceptual way of viewing the structure of CNTs has little resemblance to how CNTs are produced, however recent results show that the inverse process i.e. transforming a CNT into a graphene ribbon is indeed experimentally feasible [36, 37].

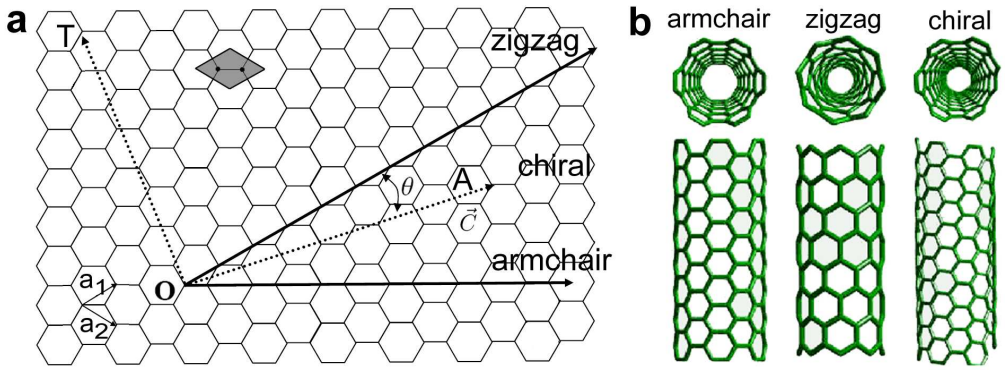

Figure 2.2: *a) Two dimensional hexagonal lattice where the basis vectors are indicated by $\vec{a}_1$ and $\vec{a}_2$. A chiral CNT is conceptually formed by cutting the lattice along the vectors OT and OA and connecting point O and A by rolling it into a cylinder. The vector $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ defines the circumference of the CNT and θ its chiral angle. The solid lines indicate the circumferences of a zigzag and an armchair CNT. The grey rhombus depicts a unit cell. b) Examples of the three different types of CNTs. Adapted from [38].*

2.2 Electronic properties of carbon nanotubes

The electronic properties of CNTs can be derived from the properties of graphene. The π bonds that originate from the p_z orbitals that extend perpendicular to the graphene plane give rise to delocalised electrons that have bands with energies close to the Fermi level. Since only electrons near the Fermi level have energies close to those of unoccupied states, these bands dominate the electrical characteristics. Therefore, the part of the band structure of graphene relevant for transport can be calculated using only the p_z orbitals ignoring the others. A tight binding calculation yields bands that are conical close the Fermi level and meet at the six K points at the corners of the Brillouin zone in reciprocal space (figure 2.3b). Only two of the six K points, denoted by K and K´, are nonequivalent and need to be considered since the others can be mapped using the reciprocal lattice vectors. However graphene has a density of states (DOS)[1] that approaches zero i.e. there are no states available for the electrons to occupy at the Fermi level which makes graphene a semimetal. In contrast, metals have

[1]The DOS describes the number of available states for the electrons for each energy interval. A high DOS means that there are many electrons with similar energies while zero DOS means that no electrons with this specific energy are allowed.

the Fermi level located within a band while semiconductors and insulators have a gap between the bands and no allowed states at the Fermi level.

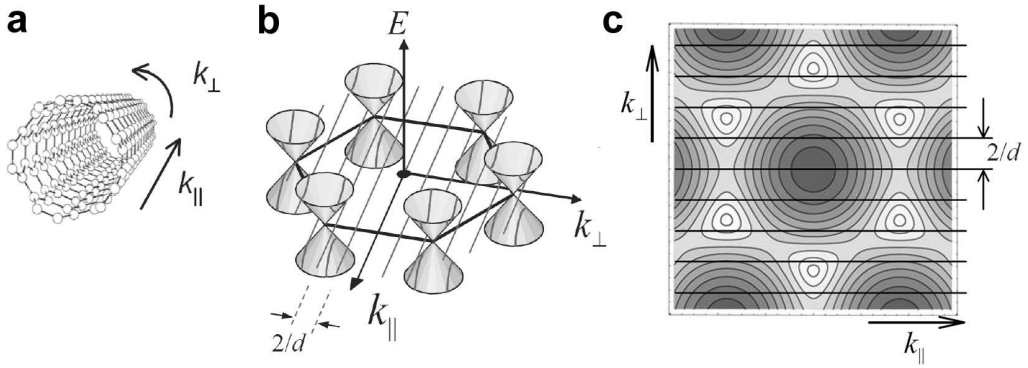

Figure 2.3: *a) CNT with arrows showing the circumferential ($k_\perp$) and tangential ($k_{||}$) directions of the electron wave vectors. b) The conical band dispersion of graphene close to the Fermi energy at the six K points. The constraints on the allowed wave vectors $k_\perp$ around the circumference induced by cylindrical wrapping of the graphene into a CNT are indicated by lines. Contour plot of the graphene band dispersion with allowed $k_\perp$ indicated by horizontal lines. Image adapted from [39].*

As a graphene sheet is rolled up into a CNT, the wavefunctions of the electrons are confined around its circumference. Since a periodic boundary condition is now imposed on the electron wave functions only discrete wave vectors that fulfill $\vec{k}_\perp \cdot \vec{C} = \pi d k_\perp = 2\pi i$, where d is the CNT diameter and i is an integer, are allowed along the circumference of the CNT. This boundary condition on the wavefunctions in a CNT gives slices of allowed k-values in the conical band structure of graphene (figure 2.3b). The position of the slices is determined by the chirality of the CNT. If a slice crosses the K and K´ points where the valence and conduction bands meet at the Fermi energy, the CNT has bands with a linear dispersion relation and is metallic (figure 2.4a). If no slice is crossing the K and K´ points the CNT has bands that are parabolic close to the Fermi level and has an energy band gap in between them i.e. it is semiconducting (figure 2.4b). The energy dispersion of the bands close to the Fermi level is given by

$$E(k) = \pm \left((\hbar v_F k)^2 + (E_g/2)^2 \right)^{1/2} \tag{2.2}$$

where $v_F = 8 \cdot 10^5$ m/s is the Fermi velocity and E_g the band gap [40]. The distance between allowed slices is inversely proportional to the diameter of the CNT which is intuitive since a small circumference gives a large

difference in the wavelengths of allowed wave functions while a large CNT has allowed wave functions with very similar wavelengths. This, in combination with the conical band dispersion, results a band gap of a semiconducting CNT which is inversely proportional to its diameter and given by $E_g = 2a_{C-C}\gamma_0/d$ where $a_{C-C} = 1.42$ Å is the nearest neighbour distance in the hexagonal lattice, $\gamma_0 = 2.9$ eV the interaction energy between carbon atoms and d the diameter giving $E_g = 0.8$ eV for a tube with a diameter of 1 nm [41].

There are also more subbands at higher energies but for CNTs with small enough diameter these do not usually influence the electronic transport properties. In 3D bulk materials the DOS increases as $\mathrm{E}^{1/2}$ which means that there are few available states close to the band edges but in 1D systems the DOS is proportional to $1/\mathrm{E}^{1/2}$ and has sharp peaks, which are known as van Hove singularities, at the edges of the bands (figure 2.4c). The DOS of CNTs has been directly measured using scanning tunneling spectroscopy by which the van Hove singularities can be clearly identified [42]. It should be noted that what are referred to as metallic CNTs are truly metallic since the DOS does not go to zero at the Fermi level as in the semimetallic graphene.

If the chirality indices of a CNT fulfill the requirement $n - m = 3p$ where p is an integer, the CNT is metallic but if $n - m \neq 3p$ it is semiconducting if only the circumferential confinement of the wave functions is considered. However, the curvature of the CNT wall induces hybridisation of the σ and π bonds which causes a band gap inversely proportional to d^2 to open up in most of the otherwise metallic CNTs [44]. This band gap is a few tens of meV for small diameter CNTs and is present in all CNTs except those with the armchair structure which are truly metallic. In such small gap CNTs there is a considerable amount of carriers thermally excited across the band gap at room temperature which gives them high conductivity and a behaviour similar to metallic CNTs. However, small band gaps in armchair CNTs were recently observed, a discovery which rivals the commonly accepted existence of truly metallic CNTs [45].

Even though both metallic and semiconducting CNTs have excellent electrical properties, the coexistence of both types has been a serious obstacle for realisation of many electronic applications that require that only one type is used. There are techniques for separating CNT material [46] and for selective growth [47] of one type of CNTs but none of these approaches have been successful enough to make CNTs competitive for large scale integration in electronics.

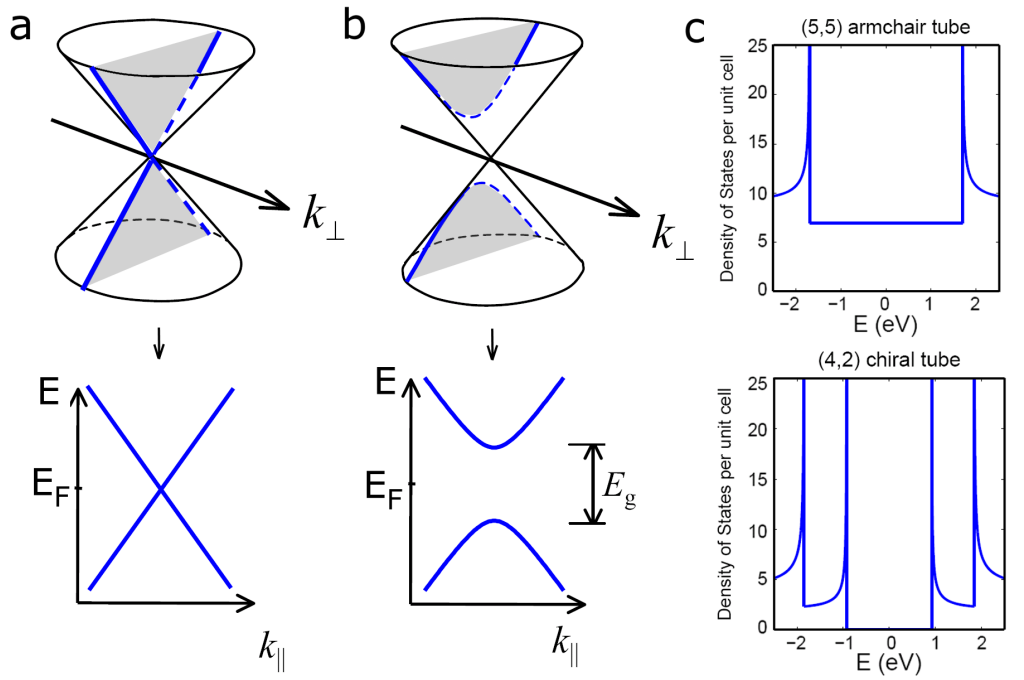

Figure 2.4: *a) The conical band structure of graphene with a slice of allowed wave vectors $k_\perp$ that goes through the point where the two bands meet at the Fermi level. This gives the 1D band structure of a metallic CNT. b) Slice of allowed $k_\perp$ not going through the point where the bands meet which gives the band structure of a semiconducting CNT. c) Density of states for a (5,5) metallic CNT with a finite DOS at the Fermi energy and a (4,2) semiconducting CNT with zero DOS around the Fermi energy. The peaks are van Hove singularities positioned at the edges of the subbands. Image adapted from [43].*

The electrical resistance in solid materials is due to scattering of electrons on static defects such as impurities and vacancies or interactions with lattice vibrations (phonons). Scattering in CNTs is different from scattering in bulk due to the lower dimensionality. In a bulk material the electrons can scatter in many different directions while in a one dimensional system they can only scatter in the forward or reverse direction giving a lower probability for scattering due to the lower number of final states available. In addition, the wave functions near the Fermi level are delocalised and extend around the circumference which means that the electrons are not strongly affected by a static defect in the CNT wall. At low longitudinal electric fields, the dominating scattering mechanism is emission of acoustic phonons with a mean free path between two scattering events of

l_{mfp} = 300 nm-1.5 µm [48, 49]. At high electric fields the electrons can gain enough energy to emit optical phonons which have a much stronger electron-phonon coupling strength and therefore a mean free path of only 15 nm [49].

Transport in one dimensional systems can be described using the Landauer-Buttiker formula which gives a conductance of $G = NT \cdot e^2/h$ where N is the number of transport channels and T the transmission probability between the source and drain contacts [50]. CNTs have two bands close to the Fermi energy at the K and K' points in reciprocal space corresponding to electrons spiraling clockwise or counterclockwise along the CNT. Each of these bands can transport one spin up and one spin down electron which gives $N = 4$. The total resistance of a CNT contacted by electrodes can therefore be written as

$$R_{tot} = \frac{h}{4e^2}\left(\frac{L}{l_{mfp}} + 1\right) + R_c \tag{2.3}$$

where L is the length of the CNT and R_c the resistance associated with Schottky or tunneling barriers at the contacts. For a device with ideal contacts ($R_c = 0\ \Omega$) and a mean free path much longer than the CNT length giving negligible scattering, the transport is said to be ballistic. If only one subband is involved in transport eq. 2.3 gives a minimum resistance of $R_{tot} = (h/4e^2) = 6.5\ \text{k}\Omega$ for a ballistic device. Measurements on short CNT segments have shown that nearly ballistic transport in CNTs is indeed possible [51].

2.3 Carbon nanotube field effect transistors

The metal-oxide-semiconductor field effect transistor (MOSFET) [52] which is the most important device for integrated circuits such as microprocessors and many memory designs, is a three terminal device which acts as a switch where the current between two of the terminals is controlled by the voltage applied on the third. In a conventional MOSFET based on Si the source and drain terminals are highly doped regions in the substrate separated by a channel region doped with an opposite polarity. A voltage is applied between the source and drain and the current between them is controlled by applying a voltage on a metallic or highly doped polysilicon gate electrode separated from the channel by a thin oxide layer. The channel is doped with an excess of electrons by donors such as phosphorous, arsenic or antimony

or with an excess of holes[2] using boron creating p-type or n-type transistors respectively.

Since the contact regions are doped with an opposite polarity compared to that of the channel, two p-n junctions connected back to back are formed. If a positive voltage is applied to the gate electrode of a n-type MOSFET the bands are bent down in the channel close to the oxide and a thin inversion layer of electrons is formed. This means that the barriers in the p-n junctions are lowered allowing transport of electrons between the source and drain through the channel.

Due to the difficulty in obtaining controlled doping of CNTs, most CNT field effect transistors (CNTFETs) use metals as contact material instead of doped regions. CNTFET devices are usually fabricated on Si/SiO_2 substrates by either using CNTs dispersed from a suspension [53] or CNTs grown directly on the sample (figure 2.5) [51]. The Si substrate which is highly conducting due to high doping serves as a back gate to which a voltage can be applied to control the current through the CNT. Even though this simple device design has proven very useful for studying the electronic properties of CNTs, the global back gate makes it unsuitable for high frequency electronic applications. Other designs have replaced the global Si back gate with local back gates of Al with natural Al_2O_3 as gate oxide [54], metal electrodes positioned close to the CNTs as side gates [55], electrolytes [56] or top gates with SiO_2 [57] or high-k [6] dielectric materials as gate oxide.

The first CNTFETs demonstrated in 1998 [53, 58] were initially assumed to operate in a similar way to conventional MOSFETs in which the electric field in the channel is the most important for controlling the transport. However, it was soon discovered that the potential barriers between the CNTs and many of the metals used dominate the transport characteristics [59]. These barriers, which exist in most metal-semiconductor contacts due to the mismatch of the work function of the metal and the electron affinity or the ionisation potential of the semiconductor, are known as Schottky barriers (SB) and are discussed in more detail in chapter 6. If the SBs are large enough, the electric field at the contacts is very important for the transport characteristics. The electric field at the contacts can be increased by decreasing the thickness of the gate dielectric or the contacts which makes the SBs thin enough to allow a considerable amount of tunneling

[2] A hole is the absence of an electron from an otherwise full valence band. Instead of considering the response of the remaining electrons to an electric field, the vacancy is treated as a quasiparticle with a positive charge.

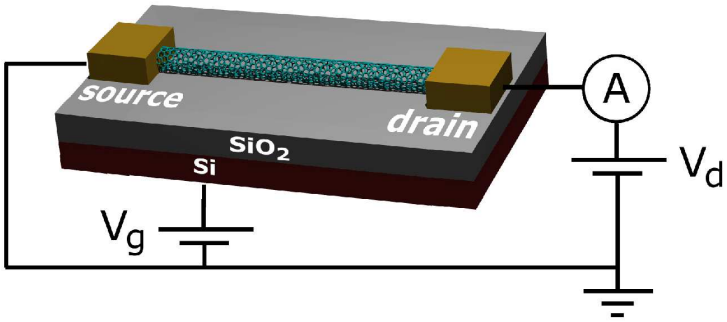

Figure 2.5: *A schematic of a back-gated CNTFET. The source is grounded and a small voltage is applied to the drain while measuring the current. A voltage applied on the Si substrate, acting as a gate electrode, is used to control the current through the CNT.*

through them [59]. The presence of SBs is a concern in CNTFETs since it limits the on-state current and deteriorates the switching since the devices require a larger change in gate voltage to change the current compared to devices without any SBs.

If a transistor is to be used for logic computation it is required that it has a large difference in current between the on and off states. If the SB for one type of carrier is increased by e.g. changing the work function of the contact metal, the SB for the other is decreased by the same amount. If the Schottky barriers for holes and electrons are similar, the device characteristic is ambipolar with high currents both for negative and positive gate voltages and a poor on/off current ratio.

The DC performance of a FET is obtained either by measuring the drain current (I_d) while sweeping the gate voltage (V_g) at a constant source-drain bias (V_d), which gives the transfer characteristic, or by sweeping V_d at a constant V_g which gives the output characteristic (figure 2.6). The transfer characteristic of a semiconducting CNT usually show a high I_d at negative V_g, a minimum at intermediate V_g and a small increase at high positive V_g (figure 2.6a). In contrast, a metallic CNT gives the same I_d for all V_g (figure 2.6c) and a semiconducting CNT with a small band gap shows an ambipolar characteristic with only a small dip in I_d at intermediate V_g since both holes and electrons can easily be transported over the small SBs at room temperature (figure 2.6d).

The characteristics of a CNTFET can be understood by studying its band

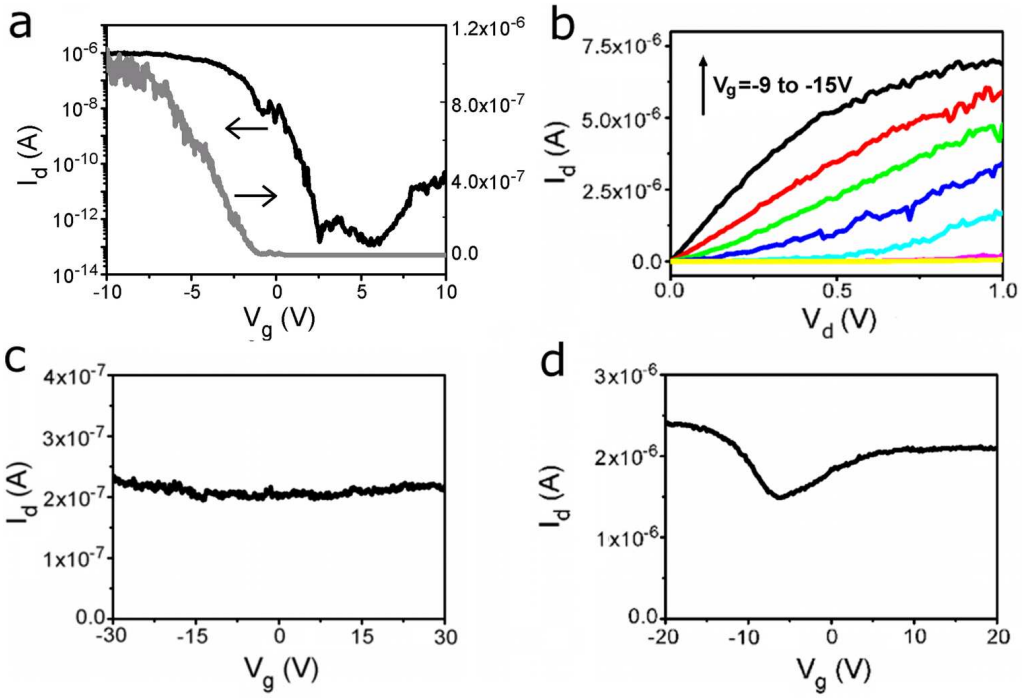

Figure 2.6: *Transfer and output characteristics of three CNTFETs. All transfer characteristics have been measured with $V_d = 100$ mV. a) Transfer characteristic of a semiconducting CNT with I_d plotted with both logarithmic and linear scales. b) Output characteristic of the device in a) at 7 different V_g. c) Transfer characteristic of a metallic CNT. d) Transfer characteristic of a small band gap CNT.*

diagram which shows the position of the top of the valence band and the bottom of the conduction band along the CNT. Band diagrams for different V_g for a CNTFET with a considerable SB height are shown in figure 2.7. As the gate electrode is negatively biased, positive holes are attracted towards it and accumulate in the CNT. This additional charge cause the valence and conduction bands to move up relative to the Fermi level in the CNT. This results in the SB for holes at the source becoming thin enough to allow for a considerable amount of tunneling (figure 2.7a). For intermediate V_g the barrier is too thick for tunneling and the only possible transport mechanism is by thermionic emission over the barrier (figure 2.7b). At high positive V_g the bands bend down making the SB for electrons at the drain contact thinner giving rise to an electron tunneling current. If the hole barrier is lower than the electron barrier the current of the p-branch at high negative V_g is several orders of magnitude larger than that of the n-branch at high

positive V_g (figure 2.6a). For a CNT with a small band gap, both hole and electron barriers are small resulting in similar currents for the p and n-branch (figure 2.6d). Applying a larger negative V_d makes the barrier at the source thinner and increases the electric field along the channel, thus increasing the current (figure 2.7d and 2.6b). For large enough V_d, the barriers are so thin that the resistance of the channel is more important than that of the contacts and at sufficiently high bias the current saturates due to phonon scattering. For intermediate V_g the current does not increase linearly with V_d at small values an indication that the SBs influence the transport.

Javey et al. have shown that it is possible to obtain CNTFETs with zero SB height for holes by using Pd contacts on large diameter CNTs [51] and Zhang et al. used Sc contacts to obtain n-type CNTFETs without barriers to electrons [61]. Such barrier-free devices have characteristics which are more similar to conventional MOSFETs since the transport is not limited by the contacts.

The ability to form both n-type and p-type transistors is crucial for computing applications where the basic building blocks are different logic gates constructed using the two types. The success of Si MOSFETs has to a large extent been due to the possibility to selectively dope the material to create both types. For CNTs, substitutional doping where the dopant atoms replace carbon atoms or interstitial doping where the dopant atoms are situated in between carbon atoms, is considerably more difficult. Doping can instead be achieved by depositing potassium atoms [62] or different molecules [63] on the CNT surface that act as electron donors through the charge transfer that occurs due to the different electron affinity of the CNT and the deposited material. Most CNTFETs exposed to air show p-type behaviour but become more ambipolar or even n-type in vacuum, an effect which has been attributed to oxygen absorbed on the CNT-metal interface when exposed to air. The oxygen changes the work function of the metal compared to its value in vacuum, shifting the energy of the Fermi level of the metal with respect to the valence and conduction band edges in the CNT and thereby altering the hole and electron SB heights [59, 62]. This mechanism has been demonstrated when removing oxygen from a CNTFET by annealing in vacuum [62]. The transfer characteristic of the device gradually changed from p-type to ambipolar and finally to n-type as the oxygen were removed. It has also been observed that a CNTFET with Pd contacts changes from p-type to ambipolar when exposed to hydrogen, an effect attributed to the lowering of the Pd work function [51]. However, the

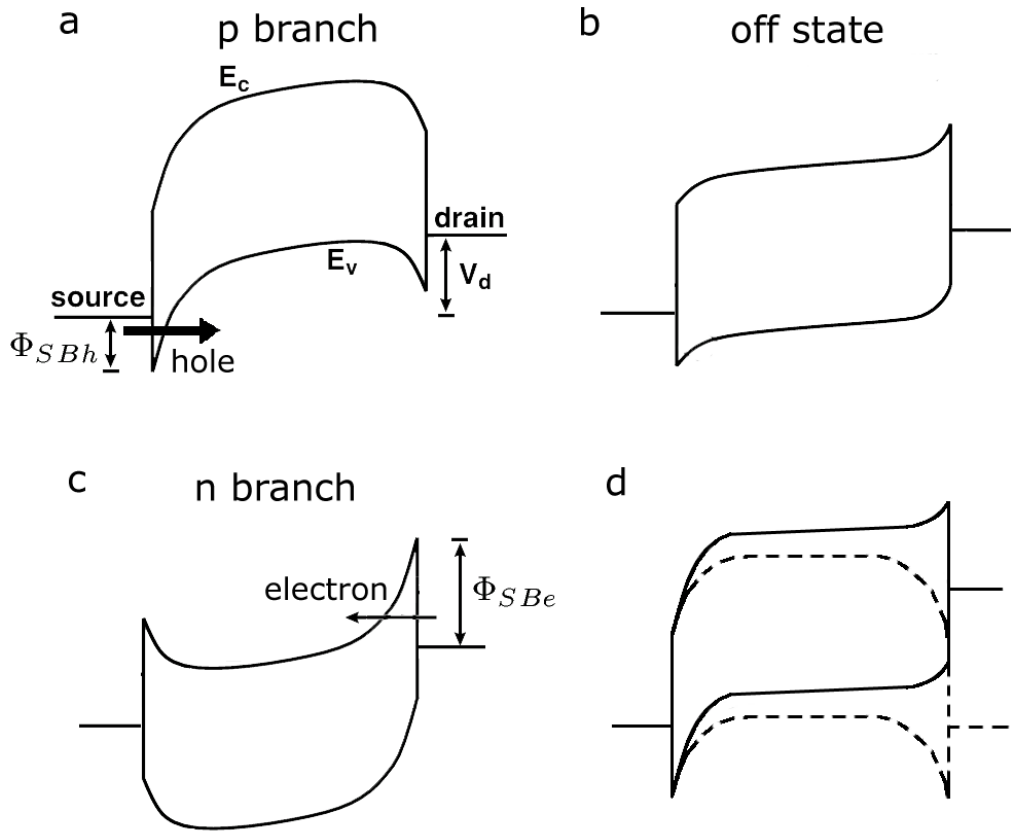

Figure 2.7: *Schematic band diagrams of a CNTFET with SBs at the source and drain contacts at different V_g and V_d. a) Low V_g with a high tunneling current of holes from the source corresponding to the p-branch in the transfer characteristic. b) Intermediate V_g at which the SBs are too thick to allow for tunneling corresponding to the minimum in the transfer characteristic. c) High V_g giving tunneling of electrons from the drain. d) Band diagrams at $V_d = 0$ V (dashed line) and at $V_d < 0$ V (solid line). The two band diagrams are shown at different V_g for clarity. Adapted from [60].*

effect of absorbed oxygen on the characteristics of CNTFETs is debated e.g it has been argued that the p-type behaviour originates from doping of the bulk of the CNT instead of a change in contact metal work function [64].

By depositing potassium or annealing in vacuum Derycke et al. have selectively n-doped a part of a CNT creating a voltage inverter which is one of the fundamental building blocks for logic computation [65]. Zhang et al. have demonstrated that both n and p-type devices can be created on the same CNT by using contact metals with different work functions which can be used to fabricate logic gates without doping the CNT [61]. Since the valence and conduction bands of CNTs are symmetric, electrons and holes have the same effective mass. This leads to similar performance for both n and p type devices which is a benefit compared to most other semiconductors where the different effective masses of electrons and holes lead to different characteristics for the two transistor types.

The main reason that semiconducting CNTs are attractive as channel material in FETs is their high mobility which is due to the small effective mass of the charge carriers and the low scattering probability which gives a long mean free path. The mobility relates the drift velocity (v_d) of the carriers to the applied electric field (E) through $\mu = v_d/E$. A high mobility implies a rapid response of the carriers to an electric field and therefore fast switching between the on and off states is obtained. For conventional semiconductors the most common method to determine the mobility is to perform a Hall measurement. However, a Hall measurement requires that contact is made to four sides of a piece of the semiconductor and is therefore impossible to implement for CNTs due to their one dimensionality. Instead, the transfer characteristic of a CNTFET can be used to obtain a field effect mobility

$$\mu_{FE} = \frac{L^2}{C_g}\frac{\partial G}{\partial V_g} \tag{2.4}$$

where L is the length of the CNT, C_g is the capacitance between the CNT and the gate and G is the conductance. The field effect mobility of a device does not only depend on the properties of the channel material but is also influenced by contact resistances, surface effects etc. For long CNTs, where the impact of contact resistances is negligible a field effect mobility of 79000 cm^2/Vs has been reported [4] which is considerably higher than the 1000 cm^2/Vs usually found for Si MOSFETs [66]. However the extracted field effect mobilities for CNTFETs have a large uncertainty since the gate capacitance is usually too small to be measurable and an idealised analytical expression is often used instead. The curvature of the bands, and therefore

also the effective mass, depends on where the slices of allowed $k_\perp$ in the graphene band dispersion are positioned (figure 2.4). Since bands closer to the Fermi level have a larger curvature, the effective mass is lower which gives a mobility proportional to the square of the CNT diameter, an effect which also has been observed experimentally [67].

Another benefit of using CNTs in FETs is their small diameter which enables good electrostatic control by a gate electrode that easily depletes the entire channel enabling devices with very short channel lengths to be operational. The potential in the channel of a FET should be fully controlled by the gate to ensure proper operation. However, as the gate length is reduced, the potential in the channel becomes influenced by the potentials in the source and drain contacts which give rise to short channel effects that are detrimental to the switching behaviour of a device. The electrostatics are improved by using a thin channel or a cylindrical gate geometry which permits a shorter gate length for a certain gate oxide thickness and therefore faster switching [68]. The large interest in using nanowires for FETs is mainly due to the improved electrostatics compared to using bulk material, however the mobility decreases for decreasing nanowire diameter due to the larger impact of scattering on imperfections at the surface [69]. In contrast, all bonds in CNTs are saturated and therefore there are no detrimental effects from surface roughness scattering.

The electrostatic control of the channel can also be improved by using a thinner gate dielectric or one with a higher dielectric constant (high-k). For conventional semiconductors it is often difficult to find a suitable high-k dielectric since many material combinations have a rough interface resulting in scattering. In contrast, CNTs are compatible with various high-k dielectrics without serious performance degradation due to the absence of dangling bonds [6].

There are a number of different metrics used to evaluate and compare the performance of FETs. Some of these that are extracted from the DC characteristics can be used to evaluate the intrinsic performance limits of a device which gives an indication of how it will behave once it is used for high frequency applications. One of these metrics is the inverse subthreshold slope, also know as the subthreshold swing, given by

$$S = \left(\frac{d log_{10}(I_d)}{dV_g} \right)^{-1}. \tag{2.5}$$

The inverse subthreshold slope is measured at the steepest slope in the transfer characteristic and describes how large a voltage change is needed

on the gate electrode to change the current by one order of magnitude. For logic computation it is required that transistors have some minimum ratio between the current in the on and the off states. Thus, it is desirable to have a low S since only a small voltage change is then needed to achieve the desired on/off ratio. This will increase the high frequency performance and lower the energy consumption in each switching event. If thermionic emission dominates transport

$$S = log(10)\frac{k_B T}{q} \cdot \frac{C_g + C_d + C_s}{C_g} \tag{2.6}$$

where T is the temperature and C_g, C_d and C_s the capacitances between the channel and gate, drain and source respectively [70]. Thus, a strong electrostatic coupling between the gate electrode and the channel is desirable since S approaches its minimum of 60 mV/dec at room temperature if $C_g \gg C_d, C_s$.

The work presented in this thesis only concerns devices with single CNTs but there are also considerable efforts being made to develop devices with multiple CNTs in the channel. Such devices are more straightforward to fabricate since they do not require knowledge of the precise position of the CNTs and therefore allow photolithography to be used. The devices give a high output current and high transconductance $g_m = dI_d/dV_g$ but on/off ratios and mobilities are lower than for single CNT devices due to the presence of metallic CNTs [71]. Therefore these devices are more suited for analogue applications where power consumption is not a major issue such as high frequency amplifiers instead of logic computation [72].

Chapter 3

Experimental Techniques

To be able to electrically characterise individual CNTs, the positions of the CNTs have to be precisely determined and metal contacts that enable connections to the measurement equipment have to be made using lithographic methods. The results presented in the appended papers have been possible due to the various techniques used to image structures with nanoscale dimensions and to fabricate structures with nanometer precision. In this chapter, the thermal chemical vapour deposition (CVD) method used to produce CNTs, the microscopy techniques used to locate and characterise them and the lithographic techniques used to contact CNTs to fabricate CNTFET devices are discussed. A more detailed description of the most important process steps in the fabrication of devices is given in appendix A. The lithographic methods used for patterning structures and depositing materials are conventional techniques which are also used in the semiconductor industry.

To characterise CNTs there are a variety of different techniques available. Several optical spectroscopy techniques such as infrared absorption [73], photoluminescence [74], Raleigh scattering [75] and Raman spectroscopy [76] can be used to probe the electronic and vibrational properties of CNTs and in some cases also be used to determine their chirality. Raman spectroscopy has been used in this work to verify that the CNTs produced are single walled (see paper I) but the main method used to characterise the CNT devices presented in this thesis is electrical measurements. Since optical microscopy can not be used to image structures which have nanometer dimensions due to the limitations in spatial resolution imposed by diffraction, other techniques have to be used to precisely locate single CNTs. Two

techniques that have been used extensively are scanning electron microscopy (SEM) and atomic force microscopy (AFM) but the CNTs have also been studied using transmission electron microscopy (TEM).

3.1 Electron beam lithography

One of the standard tools to controllably define structures in the nanometer to micrometer range is electron beam lithography (EBL). In this technique, a focused electron beam is used to expose a polymer resist which is sensitive to electrons. A planar substrate is first spin coated with a resist dissolved in a solvent whereafter it is baked to evaporate the solvent which solidifies the resist (figure 3.1b). The thickness of the film is mainly determined by the rotational speed during coating and the viscosity of the resist. Next, the resist is exposed to a beam of electrons with an energy of tens of kV (figure 3.1c). Due to the corresponding short electron wavelengths on the order of picometer, the resolution of EBL is not limited by diffraction in contrast to photolithography where photons with a wavelength of hundreds of nanometers are used to expose the resist. As a positive resist is exposed to an electron beam, its polymer chains are cut into smaller segments while the polymers in a negative resist instead are crosslinked into longer chains. The resist is exposed in a region larger than the beam size by the incident electrons due to forward scattering and the generation of secondary electrons in the resist but an even larger region is also exposed by electrons that backscatter from the substrate. Forward and backward scattering and limitations in resist resolution results in a minimum feature size of around 10 nm and a minimum spacing between features of a few 10s of nm.

After exposure, the resist is developed in a solvent which dissolves shorter polymer segments faster than long ones. For a positive resist, this leaves exposed parts of the substrate surface unprotected while other parts are covered with remaining resist (figure 3.1d). The remaining resist can be used as a mask for etching of the underlying material or for a lift-off process for deposited material. Two layers of positive resist have been used to pattern catalyst islands and metallic contacts to CNTs, a copolymer underlayer and a top layer which has a lower sensitivity than the underlayer i.e. it requires a higher exposure dose to be developed. Since the required dose is reached in a larger area for the underlayer compared to the top layer, the subsequent development results in an undercut in the resist profile. To ensure that there are no residues left in the developed areas the resist is

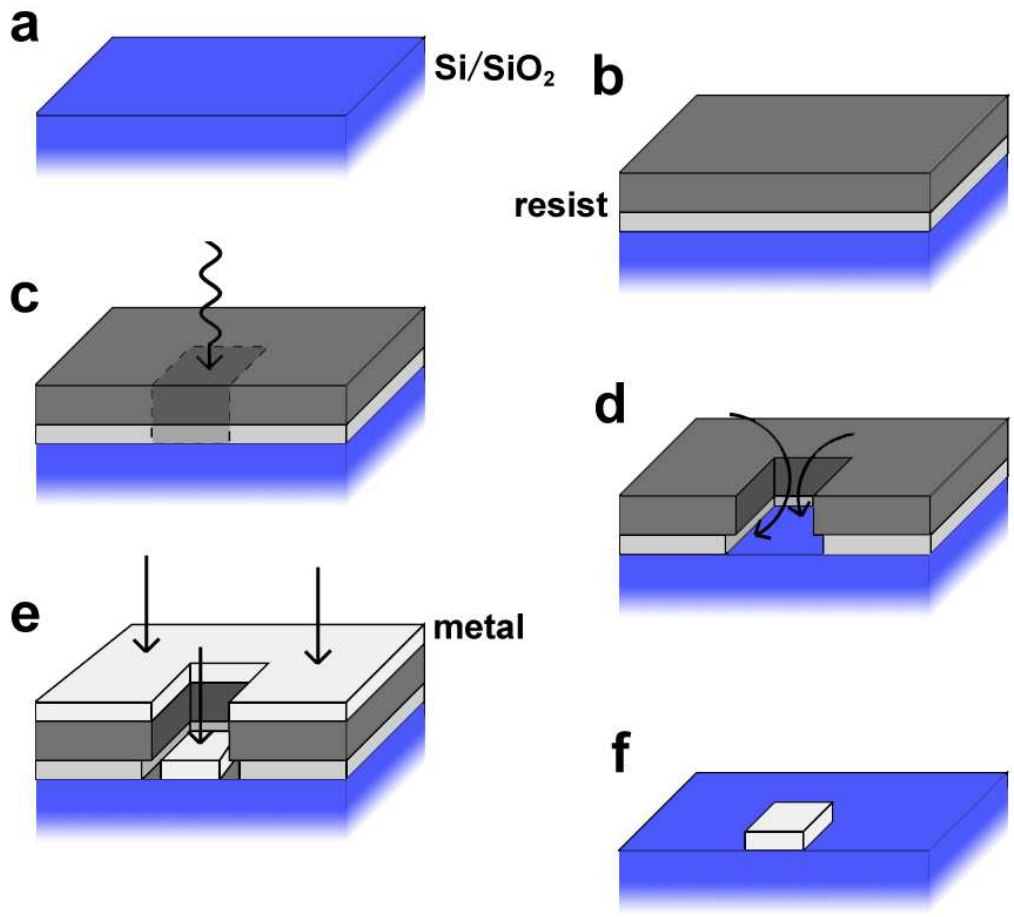

Figure 3.1: *Process steps for EBL using lift-off with a double layer positive resist. a) Si/SiO_2 substrate b) Substrate is spin coated with two layers of resist. c) Designed pattern is exposed by an electron beam. d) The exposed part of the resist is dissolved in a solvent. e) Metal is deposited using electron gun evaporation. f) The remaining resist is dissolved using another solvent leaving metal on the substrate only in the exposed areas.*

etched in an oxygen plasma. However, this process step severely damages unprotected CNTs and it therefore omitted when contacts are made.

A metal film is then deposited on the substrate using electron-gun evaporation in which energetic electrons are used to either sublimate material from a target or melt and vaporise the material. Due to the undercut in the resist profile there is a separation of the material deposited directly on the substrate and that deposited on the resist (figure 3.1e). This makes it possible to dissolve the remaining resist leaving metal only in the areas exposed by the electron beam (figure 3.1f).

3.2 Photolithography

The larger structures such as pads for electrical probing are patterned using photolithography. Instead of using electrons to expose the resist as in EBL, the substrate is illuminated by visible or UV light through a glass mask covered by a patterned metallic film that blocks the light in certain areas. In our process, the top layer is a UV sensitive positive resist and the underlayer is a resist which is unaffected by the irradiation. As the upper resist has been developed after exposure, the underlayer dissolves at a constant rate creating a resist profile where the size of the undercut necessary for lift-off depends on development time. Due to the lower exposure dose required, this resist combination has also been used for EBL of structures with sizes down to 400 nm. Photolithography has a large throughput compared to EBL since all structures are exposed simultaneously which makes it the lithography technique most suitable for mass production. On the other hand, photolithography lacks flexibility since the mask has to be defined by EBL and the pattern can not be easily modified after fabrication.

3.3 Chemical vapour deposition

CNTs are mainly produced by three different methods. The first MWCNTs were discovered in the products created in an arc discharge experiment [33]. By applying a high voltage between two graphite rods, an electrical discharge can be induced creating a plasma of carbon radicals which can form MWCNTs or SWCNTs if the rods contain some catalyst such as Ni, Fe or Co [34]. Laser ablation uses a high energy pulsed laser to irradiate a carbon

target containing Ni and Co instead of an electrical discharge to create the plasma for the CNT growth [77].

Presently, most production of CNTs is done using some variety of chemical vapour deposition (CVD) since it is a relatively simple method avoiding the extreme temperatures required in the arc discharge and laser ablation methods. Another advantage is that it is possible to grow CNTs directly at a specific position on a substrate without any need to chemically purify and disperse the material which is beneficial in the fabrication of devices with single CNTs. CVD has been known since the 1880s and is often used in semiconductor processing to deposit dielectrics and metals [78].

In thermal CVD of CNTs, carbon precursor gas molecules are dissociated at the surface of metal catalyst particles that lower the activation energy for the reaction (figure 3.2) [79]. The released carbon atoms precipitate into the particles while the rest products are transported away in the gas phase. As the particles become saturated with carbon, networks form on their surfaces or in their interiors and if the curvature of the particle is advantageous, a cap will form and lift off the surface initiating CNT growth. More carbon is added through the catalyst particles until the precursor gas flow is stopped or the particles have been coated with carbon that prevents more precursor molecules from reaching the catalyst surface. The most common carbon precursors are hydrocarbons such as methane (CH_4) [80, 81], acetylene (C_2H_2) [82] and ethylene (C_2H_4) [83] but it is also possible to use carbon monoxide (CO) or alcohols such as ethanol (C_2H_5OH) [84]. In spite of direct observations of CNT growth in TEM [85] and theoretical modeling [86, 87] the exact microscopic details of the structure of the catalyst particles and the carbon transport in them, the cap formation and the carbon incorporation into the CNTs are still not fully understood. This lack of understanding of the growth mechanisms and of what factors that are most important for successful growth is the main obstacle to the production of CNTs with defined chiralities.

The catalyst materials typically used are Ni, Fe and Co due to their ability to dissociate hydrocarbons and their high carbon diffusion rate, solubility [79] and binding strength to carbon [88] but also noble metals such as Pd and Ag can be used to catalyse the dissociation [89]. It has been shown that the diameters of CNTs are correlated to the sizes of the catalyst particles and that their diameters should be a few nanometers to produce SWCNTs [83, 90]. The catalyst particles can be prepared through chemical methods by e.g. using metal salts, metal-organic precursors or organic molecules such as ferritin to control their sizes [91, 92]. The approach used

here to produce particles for SWCNT growth is to deposit a 0.5-1 nm Fe film on a 5 nm Al_2O_3 support layer. The Al_2O_3 layer has a rough surface and strong interaction with the metal film which prevents the Fe particles from diffusing and agglomerating into larger aggregates [79]. The main benefits of using a thin metal film compared to particles prepared through chemistry are the possibility to define the position of the CNT growth on the substrate by using conventional lithographic techniques and the simple preparation method.

To grow CNTs, the substrate is placed in a quartz tube through which Ar and H_2 is flown while heating to 900°C (figure 3.2b). As the Fe film is heated it transforms into catalyst particles and when the growth temperature is reached, the Ar flow is switched to methane which is the carbon precursor used. The methane molecules are dissociated at the Fe particles and CNT growth is initiated. The yield of CNTs using this process is low which gives a small probability for bundling during growth which is beneficial for contacting individual CNTs.

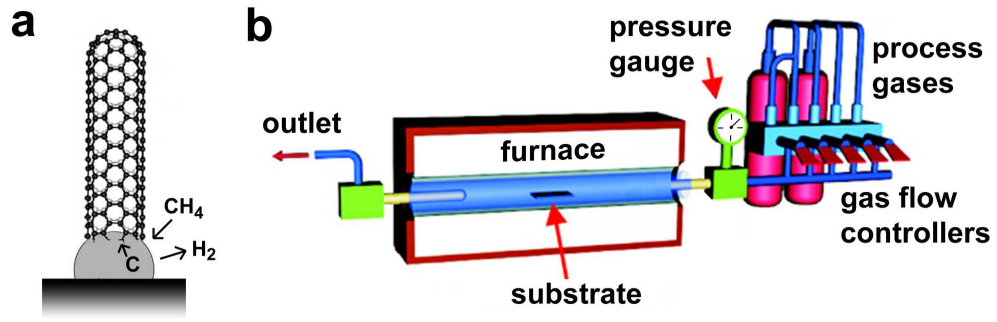

Figure 3.2: *a) Schematic of the base growth of a CNT. Methane is dissociated at the surface of a catalyst particle and the released carbon atoms are incorporated into the CNT. b) Setup for thermal CVD of CNTs consisting of a furnace enclosing a quartz tube connected to gas supplies and flow controllers.*

To ensure that the grown CNTs are predominantly single walled, they are studied using TEM, AFM and Raman spectroscopy (figure 3.3). In TEM, high energy electrons are passing through a thin sample and due to scattering an image is formed. Due to the short wavelength of the electrons it is possible to image individual atoms if abberations are corrected for. TEM is an excellent technique for studying CNTs since their walls are clearly visible and even single defects can be resolved [93]. TEM images of our material reveals that in addition to single walled there are also some double

walled CNTs produced which is not surprising since the diameters measured using AFM have a wide distribution between 0.7-4 nm in which the largest CNTs most likely have multiple walls [94] (figure 3.3b). However, most of the CNTs have a diameter less than 3 nm and the mean diameter is 1.6 nm indicating a majority of SWCNTs. Another fingerprint of the structure of a CNT is its Raman spectrum. Raman spectroscopy measures the energy shifts of photons that are inelastically scattered on a sample. This energy shift is due to the generation or annihilation of phonons that are characteristic of a material. In CNTs, the phonon energy corresponding the so-called radial breathing mode (RBM), in which the circumference expands and contracts, is inversely proportional to the CNT diameter. In addition, the intensity of the RBM is suppressed if a CNT has several walls and can thus be used to verify that a material predominantly consists of SWCNTs. In addition, the ratio between the intensities of the G-band in a Raman spectrum, which corresponds to in-plane vibrations of the carbon-carbon bonds, and the D-band, which originates from disorder in the lattice, give an indication of the quality of the CNTs since the ratio decreases with the number of defects present.

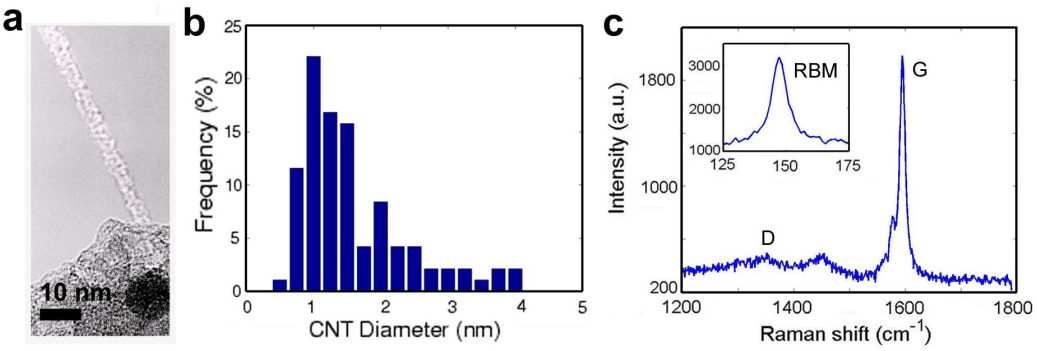

Figure 3.3: *a) TEM image of a CNT. A catalyst particle is visible in the lower right part of the image. The CNT walls are jagged due to the high acceleration voltage used which can induce defects by knocking out carbon atoms during imaging. b) Diameter distribution of 95 CNTs measured using AFM. b) Raman spectrum of an isolated CNT obtained using a 514 nm laser showing the intensity of scattered light as a function of the shift in wavenumber. The inset displays the RBM peak at 147 cm^{-1} corresponding to a diameter of 1.68 nm.*

3.4 Scanning electron microscopy

One of the simplest ways to image individual CNTs is to use a SEM. In a SEM an electron beam with a typical energy of 1-40 kV is scanned over a sample and interactions with the sample within a few nm below the surface cause low energy secondary electrons to be generated and emitted. Further down in the sample the incident electrons are also backscattered. Two different detectors can be used to image the sample using the two types of electrons since they have different energies. Since secondary electrons are more abundant than backscattered electrons and are generated closer to the surface the secondary electron emission is usually used for imaging topography. A SEM gives a contrast image, with a maximum resolution of around 1 nm, where the brightness depends on the probability of a material to generate secondary electrons when irradiated which means that e.g. a metal appears more bright than a semiconductor or an insulator.

A CNT viewed in a SEM is bright and blurry if it is lying on an insulating substrate but the contrast is more sharp if it is suspended. The reason that a SEM can be used to image CNTs even though the interaction of an electron with a CNT is small and the number of secondary electrons generated should be too few to obtain an image has been debated in the scientific literature. Explanations for the visibility of CNTs in SEM include a voltage contrast between the CNTs, that charge up slowly, and the surrounding SiO_2. Due to this voltage difference, the number of secondary electrons leaving the substrate in the vicinity of the CNTs is increased [95]. Another possibility is that the substrate loses electrons and gets positively charged which induces a flow of electrons from the CNTs locally increasing the emissivity. However, these explanations do not clarify why also suspended CNTs can be imaged using SEM. It has therefore been suggested that incident electrons passing close to a CNT induce a surface plasmon which can transfer its energy to a secondary electron and therefore increase the emissivity [96].

A concern when using a SEM to image CNTs is the possible detrimental effect on their electronic properties. It has been reported that electron irradiation of CNTs can reduce their conductance and even induce transitions from a metallic to a semiconducting behaviour [97]. However, the acceleration voltage typically used in a SEM is too low to induce structural damage by knock on collisions which require energies above 86 keV [98]. The degradation in conductance caused by SEM is also reversed with time implying that no severe structural changes have occurred but that the effect could be due to charging of the substrate surface. In our experiments, the

CNTs are imaged using a low acceleration voltage of 1 kV and at a low magnification and short exposure time to minimise the dose. CNTFETs that have been fabricated by randomly depositing contacts without prior imaging of the CNTs show very similar on-currents and subthreshold slopes as devices with CNTs that have been exposed and thus it is concluded that the SEM imaging does not cause irreversible damage to the CNTs under the conditions used.

3.5 Atomic force microscopy

In an AFM, a sharp tip with a radius of about 10 nm, attached to a cantilever, is used to image the topography of a surface. In addition, an AFM can also be used to measure other properties of a surface such as magnetic (MFM) or electrostatic (EFM) forces. An AFM can be operated in contact mode with the tip pressed against the surface, in non-contact mode with the tip far from the surface or in semi-contact mode where the tip is tapping on the surface. Semi-contact mode is the most common mode for topographic imaging since the forces between the tip and the surface are lower compared to contact mode which reduces the chance of damage but still large enough to obtain a high sensitivity compared to non-contact mode.

In semi-contact mode the cantilever is oscillated close to its resonance frequency by a piezoelectric crystal. The frequency and amplitude of the vibration is detected by a laser beam reflected off the backside of the cantilever and incident on a position sensitive photodiode. As the tip is moved in close proximity to a surface it interacts with the sample through attractive van der Waals forces and repulsive forces due to overlapping electron orbitals resulting in a reduction of the amplitude of the vibration. The cantilever is scanned across the sample surface using another piezo element while the tip-surface distance is simultaneously adjusted to give a constant vibration amplitude. By monitoring the voltage applied to the piezo needed to keep the amplitude constant, a topographic image of the surface is obtained. An AFM has a very good resolution in the vertical direction but its lateral resolution is limited by convolution due to the finite radius of the tip. This results in images where the diameters of the CNTs are exaggerated, however their diameters can still be accurately measured by studying the height difference between the CNTs and the substrate.

3.6 Electrical measurements

The electrical measurements are performed by contacting the pads connected to the CNTs with needles in a probe station. The probe station is shielded and triaxial cables are used to connect the devices to the measurement equipment to ensure a minimum of electrical noise.

For the CNT gated CNTFETs presented in paper IV and paper V a semi-automatic probe station (Cascade summit 12000) is used with the devices exposed to air during measurement. The variable temperature measurements used to extract the Schottky barrier heights between metal contacts and semiconducting CNTs presented in paper VI have been performed in a vacuum probe station (Janis ST-H-4MW-2) at a pressure of 10^{-6} mbar. The temperature of the sample can be varied from 5 to 450 K using either liquid nitrogen or helium to cool the chuck and a resistive wire to heat it.

The devices are measured using a semiconductor parameter analyser (Agilent B1500A or Keithley S4200) which is a fully integrated equipment for DC characterisation. The parameter analyser has several source-measure-units that can apply a voltage or current while measuring both simultaneously. This enables measurements of the transfer and output characteristics of the devices while monitoring e.g. gate leakage currents. The Agilent B1500A parameter analyser used for the Schottky barrier measurements has a minimum resolution of 1 fA and an accuracy of $\pm 0.46\%$ which means that the accuracy of the measurement results are not limited by the equipment but instead by noise due to transport fluctuations in the CNT devices [99].

Chapter 4

Electric field directed growth and resulting substrate deformations

Positional and directional control of CNTs is desirable since it alleviates the problem of having to locate individual CNTs to make CNTFETs and therefore enables large scale production. There are a variety of techniques to position and align CNTs deposited on a substrate from a suspension such as dielectrophoresis [100], selective adhesion on chemical groups [101] or alignment by liquid flow [102]. However, since the CNTs usually agglomerate into bundles in suspension it is difficult to use these methods to deposit separate CNTs. In addition, it is difficult to clean the CNTs from e.g. surfactants used in the suspension. It is therefore desirable to develop methods that give positional and directional control during growth. The position of CNTs can simply be controlled by lithographic patterning of the catalyst film or particles, however since it is difficult to controllably produce a single CNT from each catalyst particle the accuracy is limited. The three approaches that have mainly been used to achieve directional control during growth are gas flows alignment [103], electric field alignment [104–106] and alignment along steps on the substrate surface [107].

In this chapter, the use of an electric field applied during growth to orient CNTs for the fabrication of CNTFETs is discussed. In addition to directing the CNTs, it was found that an applied electric field can also induce deformations in the SiO_2 substrate in the vicinity of the CNTs, an effect which is attributed to Marangoni convection and capillary waves in a molten region underneath the CNTs. The electric field directed growth method is also

discussed in paper I and the substrate deformations and their formation mechanism in paper II and III.

4.1 Electric field directed growth

To obtain control of the direction of CNTs and at the same time produce straight CNTs, an electric field can be applied during CVD using electrodes patterned on the substrate [104–106] or be induced by charged catalyst islands [108]. Directional control of CNTs in an electric field is possible due to their large aspect ratios resulting in a highly anisotropic polarisability [109]. An electric field $\vec{E}$ induces a dipole $\vec{p}$ along the main axis of a CNT resulting in a torque

$$\vec{T} = \vec{p} \times \vec{E} \tag{4.1}$$

aligning the tube with the field. Due to the anisotropic polarisability, the polarisation perpendicular to the main axis can be disregarded and the magnitude of the dipole therefore simplified to

$$|\vec{p}| \approx p_z = \alpha_{zz} L E_z = \alpha_{zz} L E \cos\theta \tag{4.2}$$

where L is the length of the CNT, θ the angle between the CNT and the electric field, $E = |\vec{E}|$ is the magnitude of the electric field, p_z the dipole moment parallel to the main axis of the CNT and α_{zz} and E_z the corresponding polarisability and electric field (figure 4.1a). By combining eq. 4.1 and eq. 4.2, the magnitude of the torque can therefore be expressed as

$$|\vec{T}| = |\vec{p}| \cdot |\vec{E}| \sin\theta = \frac{1}{2} \alpha_{zz} L E^2 \sin 2\theta \tag{4.3}$$

resulting in a force that induces alignment of the main axis of a CNT along the direction of the electric field. Thus, if the main axis of a CNT is perpendicular to the electric field ($\theta = 90°$) the induced dipole moment and thus the torque is zero while if the CNT is parallel to the field ($\theta = 0°$) the torque is zero because the field and the dipole are aligned. However, CNTs with all other orientations experience a torque.

To enable the application of an electric field during growth, Mo electrodes separated by 5-80 μm gaps were patterned on a Si/SiO_2 substrate using photo or e-beam lithography and deposited using e-gun evaporation and a catalyst film was patterned either on top of the electrodes close to their edges or in the gaps. The sample was put on a quartz holder with Ta clamps

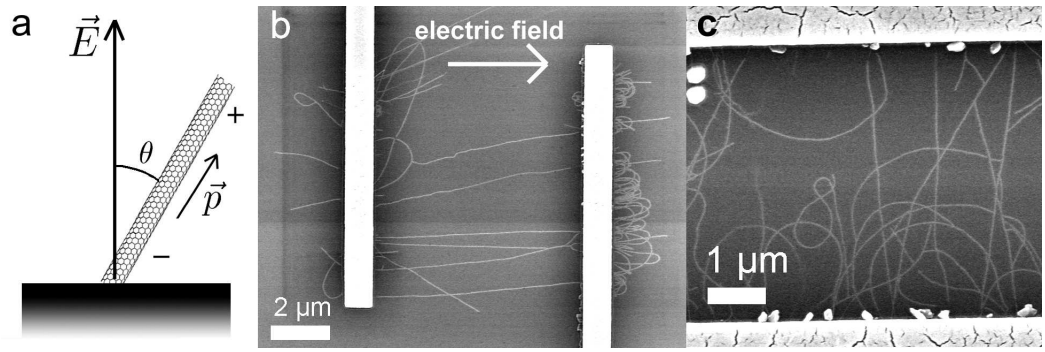

Figure 4.1: *a) Influence of an applied electric field on a CNT at an angle θ with respect to the field. A dipole $\vec{p}$ aligns the CNT with the field. b) SEM image of CNTs grown with an electric field of 1 V/µm applied in the horizontal direction. The electrodes to which the voltages are applied are not shown in the image. c) CNTs grown without any applied electric field.*

connecting the electrodes to an external voltage supply and an electric field of 1 V/µm was applied either before the methane was switched on or a few minutes after growth had been initiated. The Si substrate was kept at a floating potential or at an intermediate voltage compared to the two Mo electrodes.

If the electric field is applied before growth, CNTs originating from catalyst islands in the gaps are short since they grow in the direction of the field which is pointing along the surface of the substrate. The close distance to the surface increases the probability that thermal vibrations or disturbances in the gas flow cause the CNTs to get pinned to the substrate and stop growing. In contrast, if the catalyst is on top of the electrodes to which the voltages are applied, the electric field is instead perpendicular to the surface at the initial growth site and therefore CNTs are directed away from the surface and follow the field lines across the gaps (figure 4.1b).

CNTs grown from a negatively biased electrode in an electric field that has been switched on a few minutes after growth has started are surrounded by dark areas when viewed in a SEM. Images of the topography obtained by AFM reveal that the dark areas are deformations in the SiO_2 surface in the vicinity of the CNTs (figure 4.2). The shapes of the deformations can be roughly divided into three categories, trenches with walls surrounding the CNTs, trenches without walls and ridges. The three types of deformations can occur on the same sample and there can also be a transformation of

one type into another along the length of a CNT. In some cases there is no CNT remaining close to a deformation after growth.

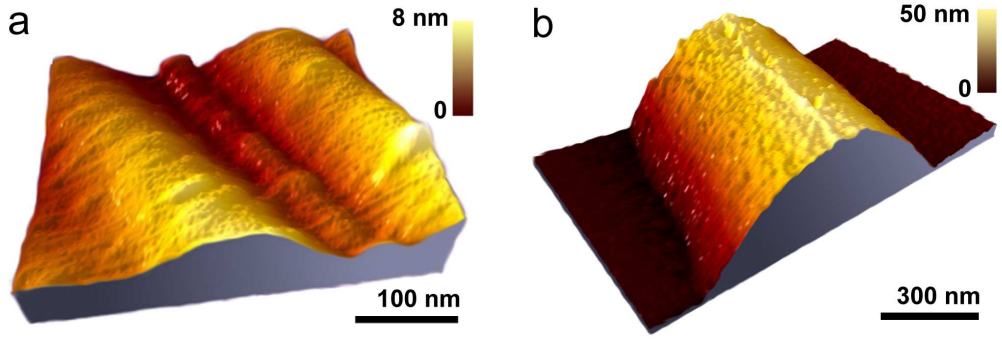

Figure 4.2: *AFM images of three types of deformations in SiO_2. a) Trench with walls surrounding a CNT. b) Ridge with a CNT on top.*

4.2 Field emission during growth

The deformations are only present around CNTs grown from negatively biased electrodes while the surface in the vicinity of CNTs grown from positively biased electrodes has no topological changes which indicates that a source of electrons is required for their formation. The electric field applied between the electrodes is 1 V/µm but due to the large aspect ratios of the CNTs, the local field around their tips is estimated using finite element simulations to be around 10^9 V/m (figure 4.3a). At such high fields, electrons can be emitted by tunneling through the potential barrier at the surface of a material, a process known as field emission [110].

A local electric field around 10^9 V/m is sufficient to obtain a field emission current on the order of microamperes from individual CNTs [111]. However, it is challenging to measure the current originating from field emission from the growing CNTs in our CVD setup since conduction through charged particles created as methane is decomposed, CNTs bridging the electrodes and carbon deposits on the substrate surface create parallel current leakage paths.

The high current through the CNTs leads to Joule heating which can raise their temperature to around 2000 K [111]. The conclusion that the CNTs reach such high temperatures during growth is supported by the presence

of deformations without CNTs remaining after growth which indicates that a too high current density has been passed through the CNTs resulting in their destruction. Due to the difference in temperature of a CNT and the surrounding environment there is a net radiative energy transfer that can be described by the Stefan-Boltzmann law and given by

$$Q_{rad} = A\epsilon\sigma(T^4 - T_0^4)t = 2\pi r L\epsilon\sigma(T^4 - T_0^4)t \tag{4.4}$$

where A is the surface area of the CNT, ϵ its emissivity, σ the Stefan-Boltzmann constant, T_0 the temperature of the environment and T the temperature of the radiating CNT, r its radius, L its length and t the growth time (figure 4.3b). For a growth time of 1200 s and an emissivity of $\epsilon = 10^{-3}$ the radiated energy is $Q_{rad} = 10^{-8}$ J.

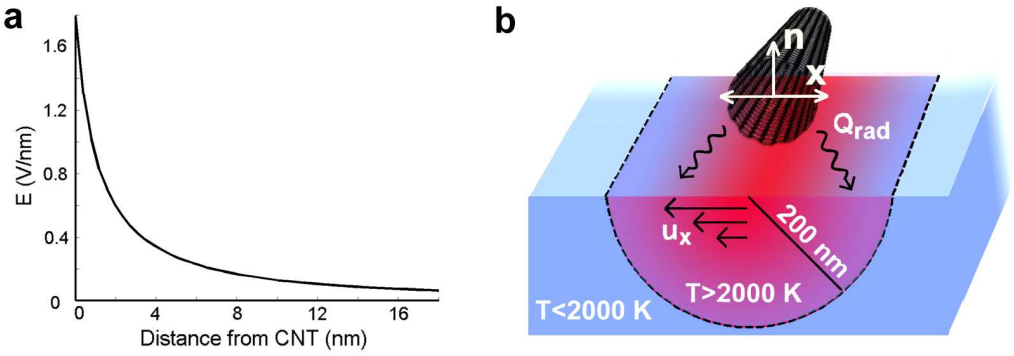

Figure 4.3: *a) Local electric field as function of distance from the tip of a CNT with a diameter of 2 nm in a gap of 10 µm at an applied field of 1 V/µm obtained using finite element simulations. b) Schematic of the radiative heating of a half cylinder of SiO_2 underneath a CNT due to Joule heating induced by field emission. Positive x is pointing away from the CNT. The horizontal velocity of the liquid u_x due to surface tension gradients is displayed as a function of depth.*

Some of the radiated energy is incident on the SiO_2 surface heating a small volume underneath the growing CNTs. The energy needed to heat a half cylinder of the SiO_2 underneath a CNT from the CVD chamber temperature of 1173 K to the melting temperature of SiO_2 of 2006 K can be estimated as

$$Q_m = \frac{\pi R^2}{2} L c_p \Delta T \tag{4.5}$$

where $c_p = 2.2 \cdot 10^6$ J/m^{3}K is the specific heat capacity of fused silica and R the radius of the cylinder. Using a radius of the melted region of $R = 200$ nm estimated from the AFM images of the deformations, the energy required

for melting is $Q_m = 10^{-9}$ J which is one order of magnitude smaller than the radiative energy emitted from the CNT. Even though the estimate is approximate since many variables are not accurately known and heat conduction through the SiO_2 and the CNTs has not been taken into account, it still indicates that Joule heating of the CNTs due to field emission is sufficient to melt the underlying SiO_2.

4.3 Marangoni convection and capillary waves SiO_2

Since SiO_2 has a poor thermal conductivity, there are large thermal gradients in the molten volume underneath a CNT. The surface tension of most liquids decreases with increasing temperature since the thermal motion of their molecules competes with the cohesive forces holding them together. Therefore, large thermal gradients also lead to large gradients in surface tension. A gradient in surface tension results in lateral transport of material at the surface towards regions of higher tension which is known as Marangoni or thermocapillary convection [112].

The more commonly observed type of fluid motion driven by temperature gradients is Rayleigh-Bénard convection where warmer liquid is moved upward and cooler liquid downward due to their difference in density. Rayleigh-Bénard convection usually dominates the behaviour of a fluid compared to Marangoni convection which is most prominent at low gravity [113], thin liquid layers or large gradients in surface tension. An occurrence of the Marangoni effect is observed in the dynamics of wine in a glass [114]. If the glass has been rotated, a thin film of wine is left on its walls. Since evaporation of alcohol occurs from all liquid surfaces the film is quickly depleted of its alcohol content due its large surface to volume ratio. Due to the removal of alcohol, the film develops a larger surface tension than the bulk liquid which causes wine to climb up the walls of the glass. As enough fluid is accumulated at some height on the wall, the gravitational force causes the wine to flow downwards again forming "tears of wine".

If there is a gradient of the surface tension s along the surface of a liquid, the vertical gradient of the horizontal component of the velocity of the liquid u_x can be described by

$$\eta \frac{\partial u_x}{\partial n} = \frac{\partial s}{\partial x} \tag{4.6}$$

where η is the viscosity, n the direction normal to the surface, x the direction along the surface and s the surface tension (figure 4.3b) [115]. Since the surface tension decreases with increasing temperature, and the temperature is reduced with increasing distance from a CNT its gradient can be expressed as

$$\frac{\partial s}{\partial x} = \frac{\partial s}{\partial T}\frac{\partial T}{\partial x} \tag{4.7}$$

where T is the local surface temperature. Since both derivatives in the right hand side of eq. 4.7 are negative, the molten SiO_2 move away from the CNT along the surface towards regions with lower temperatures. As it reaches the end of the molten region it is forced to flow downwards and back towards the hot region resulting in convective vortex motion (figure 4.4a). This convection, driven by surface tension gradients, results in a depression of the surface underneath the CNT where liquid is flowing upwards and an elevation further away from the CNT resulting in a surface profile characteristic of Marangoni convection [115, 116].

If the electric field is switched off or the CNT destroyed by excessive current through it, the molten SiO_2 cools down and the Marangoni convection is damped since the thermal gradients and therefore also the surface tension gradients are decreased (figure 4.4b). Surface tension is due to that the cohesive forces between molecules on a surface and those in the bulk results in a net force towards the bulk of the liquid which is balanced by the incompressibility of the liquid. As a flat surface is distorted, surface tension strives to minimise its area to have as many molecules in the bulk as possible. Thus, transversal capillary waves are be generated in the molten SiO_2 with the surface alternating between ridges and trenches in a way similar to the ripples generated when an object transverses a liquid surface (figure 4.4c-f). The SiO_2 surface therefore undergoes a cyclic series of structural transformations until the viscosity has increased sufficiently due to cooling so that one of the shapes is frozen into the surface. The different types of substrate deformations observed after electric field directed growth of CNTs correspond well to the different shapes that the surface go through during cooling due to capillary waves. However, some deformations consist of a ridge which is 10s of nanometers high and no visible depression of the surrounding surface (figure 4.2b). Due to the large gradients in temperature and thus viscosity of the molten SiO_2, velocity gradients can arise in the liquid. For sufficiently large velocity differences, the fluid ruptures and becomes porous. Since the ridge deformations are large and there are no suppressions of the substrate surface in their vicinity it is likely that the

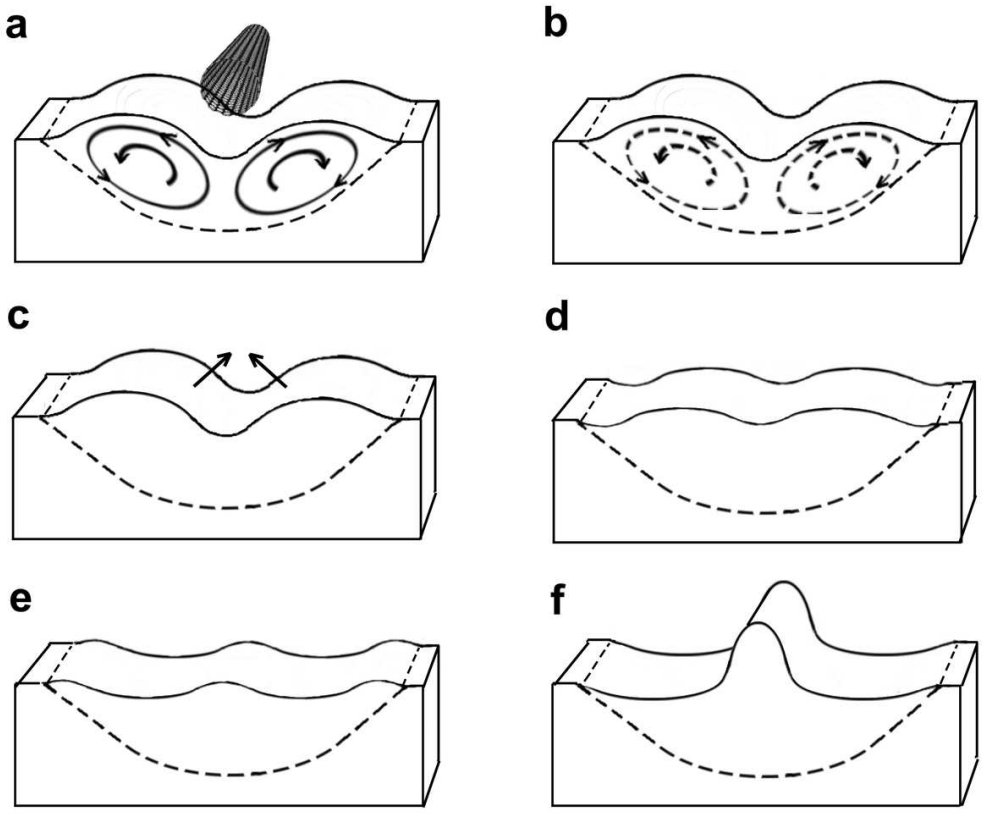

Figure 4.4: *a) Marangoni convection in melted SiO_2 due to surface tension gradients induced by local heating from a CNT. b) When the electric field is switched off or the CNT destroyed, the convection is damped due to cooling. c-f) Capillary forces that try to restore the flat surface transform the central suppression into an elevation. The sequence is repeated in reverse order (f to c). One of the profiles is solidified when the SiO_2 has increased its viscosity sufficiently.*

SiO_2 inside them is porous, a conclusion supported by the fact that they are easily destroyed as discussed in paper III.

To induce the local melting needed to produce the observed surface deformations, the CNTs need to be close to the substrate as they are growing. If the electric field is applied before growth starts, the CNTs are initially growing perpendicular to the surfaces of the electrodes since they follow the electric field lines and thus they are too far from the surface to induce melting. However, if the electric field is applied a few minutes after growth has started some CNTs will be close to the surface when the field is switched on and induce sufficient radiative heating of the substrate.

The observed deformations resemble those observed by Byon et al. who introduced a small amount of oxygen during CVD growth of CNTs [117]. Their deformations have a depression in the center surrounded by elevated ridges similar to the deformation most commonly observed in our experiments (figure 4.2a). In their experiments, most of the CNTs have been destroyed after growth and the conclusion is that carbothermal reduction, where SiO_2 reacts with the carbon in the CNTs to form volatile SiO and CO, is responsible for the trench formation. The ridges are formed because some of the evaporated material is redeposited on the surface. The main difference between the two experiments is that we do not add any oxygen during growth but a source of electrons from a negatively biased electrode is needed. It is not clear from where the energy that heats the CNTs to temperatures above 1700 °C, which is required for carbothermal reduction originates from in their experiment and why evaporated material would be deposited only around the trenches. However, it can not be ruled out that different physical mechanisms in the two experiments result in structural changes that are similar.

The deformations formed during electric field directed growth may have no direct practical applications since e.g. patterning and etching techniques using conventional lithography have superior precision and simplicity. Instead the deformations can be viewed as a manifestation of a mass transport phenomenon on a nanometer scale under somewhat unexpected conditions. In addition, the results can hopefully lead to further insights in the growth mechanisms of CNTs in electric fields [118].

Chapter 5

Carbon nanotube gated carbon nanotube transistors

The improvement in the performance of transistors is to a large extent due to the continuous down-scaling of their gate lengths resulting in higher operating frequencies. However, continuation of the gate length scaling faces considerable lithographic challenges since resist features smaller than 40 nm are required to further reduce the gate length [3]. Therefore, a method to define the gate without being limited by lithographic constraints is highly desirable. This chapter describes the fabrication and electrical characterisation of a novel CNTFET where a metallic CNT replaces the lithographically defined metal gate electrode and used to control the current through the semiconducting CNT. Two different device designs have been used. In the first design, presented in paper IV, the gate CNT is deposited from a suspension while in the second design, presented in paper V, the gate CNT is grown using CVD. The emphasis in this chapter is on details about the fabrication, the background for the numerical simulations in paper IV and a discussion of the results and a comparison of the performance with FETs using other materials or device structures.

5.1 CNTFETs with two gates

The simple back gated CNTFET described in chapter 2 has some fundamental drawbacks that deteriorate the performance as device dimensions

are scaled down and that makes it incompatible with high frequency operation. To obtain a low inverse subthreshold slope in a CNTFET with a finite Schottky barrier (SB) height, the SB thickness has to be modulated efficiently by the field from the gate electrode. By making the gate dielectric thinner the control can be improved, but this also results in a higher off current and more ambipolar transfer characteristic due to the thin barrier for electrons at the negatively biased drain electrode [119]. It is possible to reduce the impact of the gate field at the drain contact by only partially gating the CNT close to the source which lowers the electron injection, however this approach is not scalable to small device lengths due to fringing fields that affect also the drain contact [120]. Another approach is to selectively dope segments of the CNT that are close to the source and drain electrodes and use a central gate to modulate the potential only in the middle of the CNT (figure 5.1). The doping can be done chemically using alkali metals [65] or polymers [121] or electrostatically using an additional gate electrode [122, 123]. If the contact regions are doped p-type, holes are easily injected from the source contact due to the thin SB while electrons injected from the drain have to be thermionically emitted over a high barrier consisting of both the SB and an additional barrier induced by doping. The device has therefore a more unipolar characteristic compared to a device with a single gate. The operation of a CNTFET with doped segments is similar to a conventional MOSFET in which the source and drain are heavily doped and thermionic emission over the potential barriers in the p-n junctions determines the transport. By using doped regions the transport is modulated by thermionic emission over a central barrier instead of tunneling through the SBs at the contacts and thus a smaller inverse subthreshold slope can be obtained than for a device with a single gate. In addition, since the device is switched by changing the potential in the bulk of the CNT, the characteristics are less dependent on the properties of the metal-CNT contact which can differ considerably from device to device [124].

The most straightforward method to create electrostatically doped segments is to use a fixed voltage applied to a global back gate to dope the regions close to the contacts and a local gate positioned in the center of the CNT to switch the device. The central gate can either be on top of the CNT so that the channel is sandwiched between the gates or be positioned underneath the CNT channel. Since the potential in the bulk part of the CNT should ideally be controlled by the central gate without any influence of the field from the back gate it is beneficial to have the two gates on the same side of the CNT since the central gate effectively screens the field from the

back gate in this configuration. Most dual gated CNTFETs use a metal

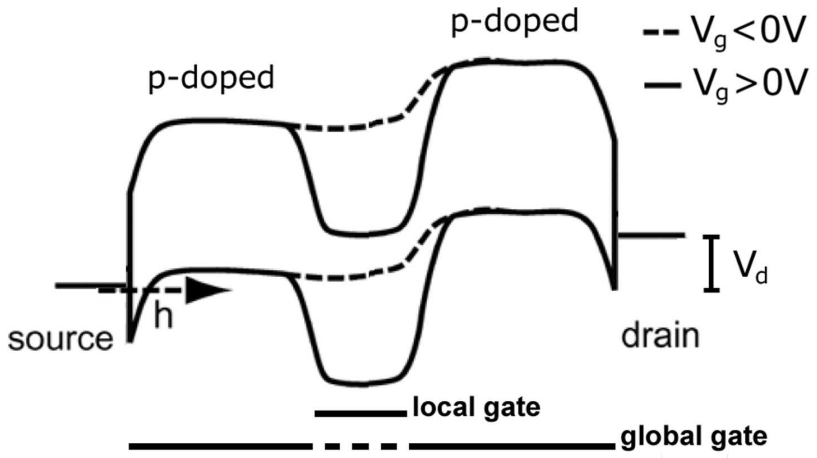

Figure 5.1: *Schematic band diagram of a dual gate CNTFET where a negative voltage applied to a global gate is used to p-dope regions close to the contacts allowing holes to tunnel through the SB at the source. The transport is controlled by changing the voltage applied to a local gate electrode that modifies the height of a barrier over which holes are transferred by thermionic emission. Adapted from [123].*

strip as the gate electrode limiting the minimum gate length by constraints imposed by lithography. In our devices, the metal gate is replaced by a metallic CNT which gives a gate length much shorter than what can be achieved through lithographic techniques since it is defined by the CNT diameter (figure 5.2a).

Metallic CNTs have excellent electrical and thermal conductivity and are investigated as a possible replacement for metals as interconnects in integrated circuits. As the packing density in integrated circuits is increased, the size of the interconnects between the transistors has to be reduced leading to current densities high enough to cause migration of metal atoms eventually resulting in discontinuities in the wires. Another problem with conventional metals is that their resistivity increases with decreasing cross section due to the increased fraction of scattering that occurs at the surface. The use of metallic CNTs eliminates both of these issues since they can withstand 1000 times higher current densities (10^{10} A/cm^2) compared to Cu wires without breaking and surface scattering is absent [5]. However, in spite of their excellent properties and demonstrated high frequency performance in the GHz range [125] it has proven difficult to integrate

metallic CNTs in interconnects where many parallel CNTs are needed due to their low packing density giving a too low current density to compete with conventional metals. Even though there are still difficulties realising CNT interconnects for larger currents, a single metallic CNT is sufficient as a gate electrode for a CNTFET with a semiconducting CNT as channel.

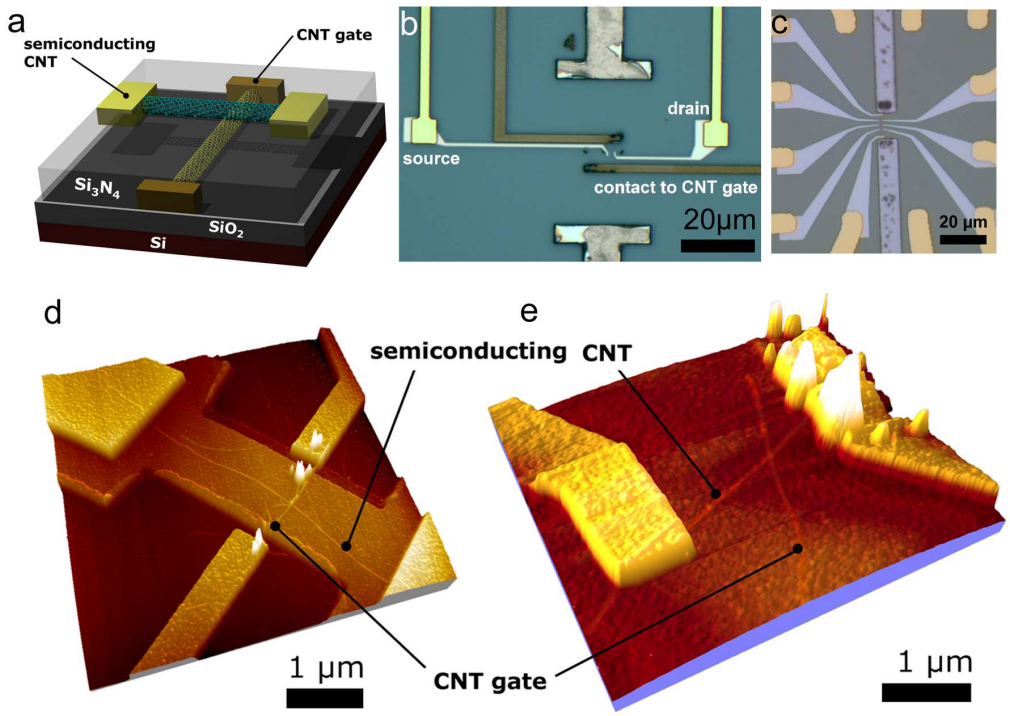

Figure 5.2: *a) Schematic of a CNT gated CNTFET where the metallic CNT gate is positioned underneath the Si_3N_4 dielectric separating it from the upper semiconducting CNT. b) Optical microscopy image of a device with the design shown in a). Upper and lower T-shaped electrodes are used to apply an electric field during growth. The L-shaped electrodes are Mo contacts to gate CNTs. The Pd electrodes that contact the semiconducting CNT are seen in between the Mo electrodes. c) Optical microscopy image of a device where the CNT gate is deposited on top of the dielectric using dielectrophoresis. In this device three CNT gates can be deposited using the six side electrodes. d) AFM image of a device with the CNT gate on top of the Al_2O_3 gate dielectric. e) AFM image of a device with the CNT gate underneath the Si_3N_4 gate dielectric.*

Previously, deposited bundles of CNTs both for the channel and the gates have been used to fabricate CNT gated CNTFETs [126]. Since the bundles are large, the gate length is around 50 nm which can easily be achieved

using lithography, and due to the presence of metallic CNTs in the bundles the on/off ratio of these devices is only around 10. CNT gated devices without using a gate dielectric between the CNTs have also been fabricated by moving the gate CNT in close proximity to a semiconducting CNT through manipulation with an AFM [127]. The transfer characteristic obtained by sweeping the CNT side gate displays a five times lower inverse subthreshold slope than the back gate sweep. However, it is difficult to fabricate devices reproducibly with a controlled distance between the CNTs using this technique. In another method to produce CNT gated CNTFETs, CNTs are deposited on a DNA template [128]. Using this technique it is possible to form crossed CNTs with the DNA template acting as a gate dielectric in between. However, a device fabricated using this technique shows a high resistance and poor switching and it can also not be ruled out that the metal contact to the gate CNT is influencing the potential of the channel since the distance to it is only few tens of nanometers.

5.2 Fabrication of CNT gated CNTFETs

Two different approaches have been used to fabricate the CNT gated CNTFETs presented in this thesis. The first device designs used dielectrophoresis to deposit the metallic CNT gate on top of a dielectric separating it from the semiconducting channel CNT as described in paper IV. However, due to poor control of the deposition and the unfavourable electrostatics of the resulting device, a second design has been developed where the dielectrophoretic deposition of the CNT gate was replaced by a second CVD step giving simpler fabrication, shorter gate lengths and also enabling devices where the CNT gate is positioned underneath the semiconducting CNT as described in paper V. Since the fabrication of the CNT gated CNTFETs is only briefly discussed in paper IV and paper V, this section is devoted to a more in depth description of the different steps and particular emphasis is on the dielectrics and deposition methods that have been tested throughout the development of the two different devices. Detailed descriptions of the most important process steps can be found in appendix A.

CNTFETs with deposited CNT gates

The fabrication of both types of devices starts with the growth of the lower CNT using CVD as described in chapter 3.3. In devices with the first design

where the CNT gate is deposited on top of the dielectric, suitable CNTs are located using AFM or SEM and Pd source and drain contacts are patterned and deposited on them. Next, the gate dielectric that separates the semiconducting channel CNT from the metallic gate CNT is deposited. The deposition of the gate dielectric is one of the most crucial steps in the device fabrication and a few different techniques have been tested to identify which one causes the least degradation of the electrical properties of the CNTs and is compatible with the subsequent processing steps. SiO_2 has been deposited using plasma enhanced CVD (PECVD) using SiH_4 and O_2 as precursors, electron gun evaporation or reactive sputtering of Si in an oxygen atmosphere. After using any of these deposition methods the contact between the source and drain electrodes is often lost. It is likely that the ionic oxygen species formed in the plasma during PECVD and sputtering cause severe damage by reacting with defects in the CNTs resulting in many broken devices. In spite of the poor yield of devices surviving SiO_2 deposition by electron gun evaporation, it has successfully been used to make the devices presented in paper IV. Al_2O_3 produced by repeated thermal evaporations of thin Al layers with oxidation in air in between has also successfully been used as gate dielectric. However, we have found that the deposition method for Al_2O_3 most benign to CNTs is atomic layer deposition (ALD) which is a chemical deposition method that can be used to deposit a variety of oxides, nitrides, III-V compounds and a few noble metals. For deposition of Al_2O_3 the substrate is heated to 150°C and alternately exposed to trimethyl aluminum (TMA) and water. ALD enables controlled deposition of single monolayers due to the self limiting nature of the chemical reaction and does not damage the CNTs since the oxidation of Al is done by water and no oxygen radicals are present. We have used devices with Al_2O_3 deposited using both of these methods to study the formation and manipulation of multiple quantum dots in series along semiconducting CNTs [129]. However, a detailed description of these experiments is beyond the scope of this thesis.

After the dielectric deposition, Pd electrodes that are used for the deposition of the gate CNTs by dielectrophoresis are patterned on both sides of the CNTs (figure 5.2c). A small drop of CNTs dispersed in Sodium dodecyl sulfate (SDS) is deposited on the chip while an alternating electric field of 2-4 V/μm is applied between the electrodes for 5-30 s after which the chip is rinsed with water. CNTs that have moved to the gap between the electrodes are pinned due to van der Waals interactions with the surface and are thus not removed during the water rinse. A resulting device with evaporated Al_2O_3 as the gate dielectric is displayed in figure 5.2d. This device

has a bundle of CNTs deposited instead of a single tube. The reason for this could be that some bundles are present in the suspension or that multiple CNTs are deposited forming a bundle on the surface. The deposition of a single CNT using DEP is difficult since the process is very sensitive to CNT concentration and deposition time. The gate length is therefore considerably longer than the diameter of a single CNT which limits the performance of the device.

CNTFETs with CVD grown CNT gates

In the fabrication of the devices with the CNT gate positioned underneath the gate dielectric used in paper V the first CNTs are grown using CVD while an electric field is applied to obtain orientational control as described in chapter 4. Instead of locating the grown CNTs after this step, as for the devices with a deposited CNT gate, large Ti/Mo electrodes are patterned that cover the catalyst areas and thereby contact several CNTs. Since a second CVD step is needed to produce the upper CNTs, a gate dielectric that can withstand the high temperature and highly reducing atmosphere during growth is needed. The Al_2O_3 deposited by ALD was found to be incompatible with the conditions used during CVD and electrical shorts through the SiO_2 to the back gate were formed. The shorts only occurred when methane was present and not when the sample was heated only in Ar. Since Al_2O_3 has a high melting point of 2072°C and thus should be able to withstand the 900°C used during growth it seems like the highly reducing atmosphere during growth damages the film. Nevertheless, the reason for the leakage through the 400 nm thick SiO_2 is unclear.

Due to its poor stability, Al_2O_3 was replaced by Si_3N_4 deposited by PECVD in the second device design. The sample is heated to 300°C during PECVD and therefore water and oxygen molecules absorbed on the CNTs and the contacts evaporate and the subsequent deposition of Si_3N_4 passivates the devices preventing further absorption when exposed to air. The PECVD process causes the transfer characteristic of the semiconducting CNTs to change from p to n-type after deposition (figure 5.3a). Previous studies have reported that depositing Si_3N_4 on only the contacts results in n-type devices which are stable in air so the change in characteristic after deposition can be attributed to a change in work function of the contact metal instead of a change in doping of the CNT [130]. A large hysteresis in the transfer characteristic of several volts for different directions of the gate voltage sweep is

present, an observation commonly attributed to charge traps in water molecules or silanol groups on the SiO_2 surface [131, 132]. The hysteresis has decreased slightly after Si_3N_4 deposition indicating that some charge traps have been removed. Even though molecules absorbed on the surface have been removed by the heating, it is possible that other charge traps present in the Si_3N_4 are responsible for the remaining hysteresis [133]. Apart from changing the characteristic of semiconducting CNTFETs, the deposition of Si_3N_4 has no detrimental effect on device performance with a high yield of devices that survive the process and metallic CNTs that show negligible change in resistance after deposition. Suitable devices where CNTs from

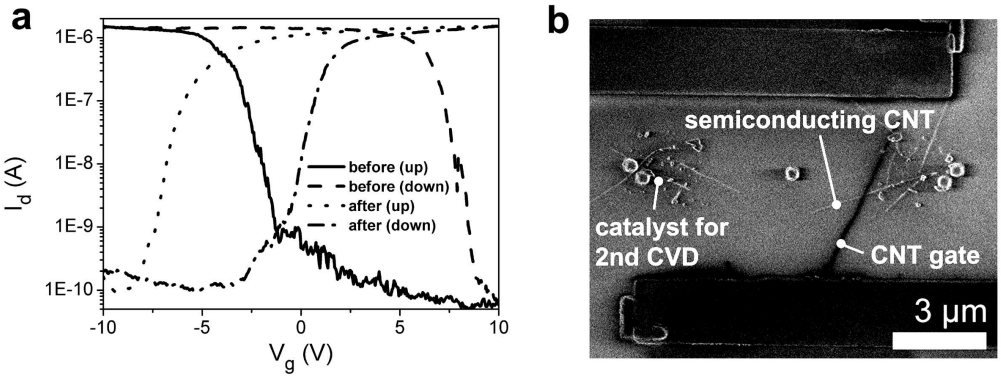

Figure 5.3: *a) Transfer characteristics with $V_d = 1$ V before and after Si_3N_4 deposition by PECVD with different directions of the gate voltage sweep. b) SEM image of a CNT gated CNTFET before contact to the CNT on top of the gate dielectric is made. The dark vertical CNT is below the Si_3N_4 and the bright CNTs are on top of it. The upper and lower horizontal electrodes are the contacts to the lower CNTs used as gates.*

the first and second growth steps are crossing are located with respect to Mo markers using SEM (figure 5.3b). The CNTs that are underneath the Si_3N_4 have a dark contrast while the CNTs on top have a bright contrast with respect to the substrate when imaged using SEM, an effect which could be due to different charging of the CNTs. Even though AFM gives a more precise location of the CNTs compared to SEM it is difficult to use since the magnitude of the roughness of the Si_3N_4 surface is similar to the CNT diameter. Finally, the upper CNTs are contacted by Pd electrodes using EBL and Ti/Au pads are made using photolithography to enable electrical probing. Since the lower CNTs and their Mo contact electrodes are covered by Si_3N_4, areas on the Mo pads are defined by photolithography and selectively etched by a CF_4 plasma using reactive ion etching.

5.3 Modeling of transport in CNTFETs

Numerical simulations have been performed by Yury Tarakanov at Chalmers University of Technology to gain an understanding of the transport characteristics of our devices and to identify possible improvements to the device design. A detailed description can be found in Yury's Licentiate thesis [134] but a brief introduction to the simulations is presented in this section. It is challenging to theoretically treat all aspects of transport in a CNTFET in detail. A detailed description requires an atomistic description of the nanotube, its contacts and surrounding dielectrics together with quantum mechanical treatment of electron transport using both ballistic and diffusive mechanisms. Such modeling requires huge computational resources so simplifications are usually made and parameters extracted from experiments are put into the calculations. Many approaches use an idealised cylindrical geometry with a gate electrode that wraps around the CNT [135] to reduce the dimensionality of the problem. However, due to the complex geometry of the CNT gated CNTFETs, such simplifications can not be made and the full three dimensional electrostatics has to be taken into account.

For short CNTs with little scattering in the channel, a quantum mechanical description is often used that involves solving the Schrödinger equation for the electrons [68]. Since our devices have lengths on the order of μm which is longer than the mean free path for scattering, they are modeled using diffusive transport in the bulk of the tube while the contact regions are treated quasi-classically (figure 5.4b).

The following section describes the principles of the modeling of CNTFETs using a device with a single gate as an example. As mentioned in chapter 1 and discussed in more detail in chapter 6, a SB is formed when a metal and a CNT are joined. Carriers are injected from the metal into the CNT either by tunneling through the SB or, if they have sufficient energy, by thermionic emission over it (figure 5.4a). A negative voltage applied to the drain raises the Fermi level in the bulk of the CNT above the Fermi level of the source which is grounded. By applying a negative voltage on the gate, the bands in the CNT are raised which moves the valence band closer to the Fermi level. Due to the Fermi level mismatch, the number of holes at a specific energy is larger in the metal than in the CNT so they are therefore transported into the CNT. Our experimental devices have Pd as contact metal resulting in a hole barrier much smaller than the electron barrier due to its high work function of 5.12 eV. Therefore, the electrons injected from the negatively biased drain electrode are disregarded in the calculations.

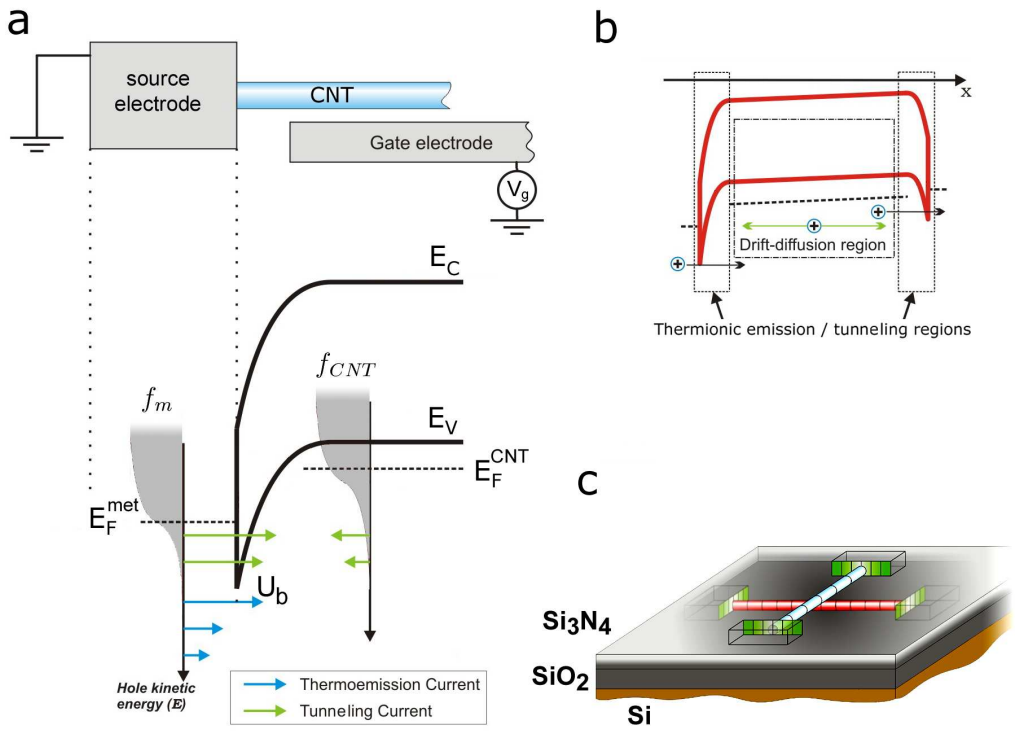

Figure 5.4: *a) Schematic of the contact between a metal and CNT with a finite SB in the vicinity of a gate electrode and the corresponding band diagram with a negative voltage applied on the gate. The hole distributions in the contact (f_m) and CNT (f_{CNT}) are displayed where the grey shaded area corresponds to filled states. b) Band diagram for a CNTFET with a negative gate voltage and a small voltage applied between source and drain. The division of the CNT into injection and diffusive regions is indicated by boxes. c) The meshing of the device into surface elements each with a constant potential. The two CNTs are divided into cylindrical elements and the surfaces of the electrodes into rectangular. The dielectric interfaces are only included schematically, the effect of these on the capacitances are taken into account by image charges that are not shown.*

The injection current is obtained by multiplying the difference between the hole distribution in the metal (f_m) and the distribution in the CNT (f_{CNT}) with an energy dependent transmission probability $T(E)$ and the DOS and integrating over energy. For holes that have an energy lower than the top of the SB and are injected by tunneling, the net current is given by

$$I_h^{tun} = \frac{4e}{h} \int_{E_{min}}^{U_b} T(E)(\overbrace{f_m(E - E_F^{met})}^{metal \to CNT} - \overbrace{f_{CNT}(E - E_F^{CNT})}^{CNT \to metal}) \, dE \tag{5.1}$$

where E_{min} is the lowest energy at which a hole can tunnel into the CNT corresponding to the top of the valence band in the bulk of the CNT, U_b the energy at the top of the SB, E_F^{met} the Fermi level in the metal and E_F^{CNT} the Fermi level in the CNT. Holes with an energy higher than the SB height which have a transmission probability of $T(E) = 1$ give rise to a net thermionic emission current

$$I_h^{TE} = \frac{4e}{h} \int_{U_b}^{\infty} \left(f_m(E - E_F^{met}) - f_{CNT}(E - E_F^{CNT}) \right) \, dE. \tag{5.2}$$

A similar treatment is performed for the other contact where holes are injected into the negatively biased drain from the CNT. In the bulk part of the CNT, the transport is described using drift which is transport due to an electric field, and diffusion which is transport due to a gradient in carrier concentration. Our model describes the operation of a CNTFET at sufficiently negative gate voltages to have the Fermi level close to or in the valence band resulting in negligible electron concentrations so recombination can be disregarded. The change in the concentration of holes per unit length, at a position x along the CNT at a time t, given by $p(x,t)$ has to satisfy the continuity equation

$$\frac{\partial p(x,t)}{\partial t} = -\frac{1}{e} \frac{\partial I_p(x,t)}{\partial x} \tag{5.3}$$

where $I_p(x,t)$ is the local hole current. The current is given by the drift-diffusion equation

$$I_p(x,t) = \overbrace{ep(x,t)v_p(F_x,p)}^{drift} - \overbrace{eD_p(F_x,p)\frac{\partial p(x,t)}{\partial x}}^{diffusion} \tag{5.4}$$

where $v_p(F_x,p)$ is the drift velocity of the holes, which depends on the electric field F_x and the hole concentration, and

$$D_p(F_x,p) = \frac{k_B T}{e} \frac{v_p}{F_x} \tag{5.5}$$

is the diffusion coefficient. The first term in eq. 5.4 describes the response of the holes to an electric field and the second term is the response of the holes to a gradient in carrier concentration. The drift velocity is related to the mobility μ by

$$v_p = \mu F_x \tag{5.6}$$

where the mobility for CNTs at low electric fields is

$$\mu = \frac{2ev_p}{\pi\hbar}\tau_0 \cdot \frac{\left(\frac{3\pi d}{8}\right)^2 p}{1 + \left(\frac{3\pi d}{8} p\right)^2} \tag{5.7}$$

where τ_0 is the time between scattering events and d is the CNT diameter [67]. At electric fields higher than 1 V/µm the drift velocity saturates due to optical phonon scattering, an effect which is included in the calculations by assuming a constant F_x at high enough bias.

To obtain the current through the semiconducting CNT the electric field along the channel CNT F_x, which is the gradient of the electrostatic potential, has to be calculated. Since the CNT gated CNTFET has a quite complicated geometry there are no analytical solutions to obtain the electrostatic potential in the devices but instead numerical calculations have to be used. The electrostatic potential φ at position $\vec{r} = (x, y, z)$ is related to the charge density $\rho(\vec{r})$ by the Poisson equation

$$\nabla^2\varphi(\vec{r}) = -\frac{\rho(\vec{r})}{\epsilon_s} \tag{5.8}$$

where ϵ_s is the permittivity. Eq. 5.8 is solved using the boundary element method (BEM) which approximates solutions to partial differential equations by calculating values only at discrete points of an object [136, 137]. Since charges in metals are located at their surfaces, BEM is the most suitable method since it does not use any points inside the electrodes or in empty space but instead only calculates the charge densities on surface elements. This simplification reduces the number of points needed in the calculation which therefore requires less computational resources. The impact of the dielectrics on the capacitances between the CNTs and the source, drain and gate electrodes is taken into account by using image charges instead of calculating the charge density on a large planar mesh at the dielectric interfaces, a simplification which further reduces the computational load.

The calculation is initiated by dividing the CNTFET into discrete surface elements and applying some voltages to the source, drain and gate electrodes

and adding some charge concentration on the CNT. The electrostatic potential in the semiconducting CNT and the charges on the electrodes, obtained by solving the Poisson equation (eq. 5.8), are used to calculate the electric field. The drift velocity and diffusion coefficient calculated using eq. 5.6 and eq. 5.5 are then inserted in the coupled continuity (eq. 5.3) and drift-diffusion (eq. 5.4) equations to obtain the current. Time is propagated and the current give rise to a new charge distribution in the subsequent time step which is inserted in eq. 5.8 to obtain a new potential distribution. This procedure is repeated until the change in the charge distribution is negligible i.e. a steady state has been reached. By calculating the charge distribution and current for different back gate or CNT gate voltages the transfer characteristic using either of the two gates are obtained.

5.4 Results from electrical measurements and simulations

The devices are electrically characterised in a probe station as described in chapter 3 by grounding the source, applying a fixed voltage on the drain and keeping one of the gates at a fixed negative voltage while sweeping the other.

For devices where the gate is a bundle of CNTs deposited by DEP as in paper IV the voltage on only one of the gates was swept while the other was kept on a floating potential. Nevertheless, the CNT gate can be used as a gate, possibly because the SDS solution used during DEP chemically dopes the contact regions which for this device are not covered by the dielectric. The device shows no improvement of the characteristic when using the CNT gate compared to the back gate. Since the device exhibited poor characteristics an improved fabrication method was developed that includes two CVD steps as discussed in paper V. Devices produced using this method is therefore the main focus of this chapter.

The device presented in paper V has only one contact to the gate CNT (figure 5.3b) and thus it is not possible to deduce whether the gate CNT is a metallic or a semiconducting CNT. However, a small back gate voltage is sufficient to induce the charge density needed on a semiconducting gate CNT to be able to use it efficiently. An applied voltage on the upper Mo electrode which is not connected to the gate CNT does not influence the

conductance of the channel CNT which proves that it is not the metal electrodes that gates the CNT since they are too far from it to be effective.

Electrical measurements reveal that the CNT gate switches the device more efficiently than the back gate with a 2.6 times lower inverse subthreshold slope (figure 5.5a). The lower inverse subthreshold slope can be attributed to that the thick dielectric of 1 µm SiO_2 used for the back gate causes it to have a weaker coupling to the channel compared to the CNT gate with a 30 nm Si_3N_4 dielectric. Moreover, the back gate switches the device by controlling the tunneling currents through the SBs at the contacts in addition to controlling the potential in the bulk of the CNT channel, which increases the inverse subthreshold slope compared to exclusive bulk switching [124]. That the inverse subthreshold slope using the CNT gate is far from the 60 mV/dec expected for thermionic emission can be explained by the fact that the gate dielectric is still quite thick and that charge trapping could be degrading the performance [138].

For a device which has a semiconducting CNT with a large band gap, such as the one presented in paper V, the transfer characteristic is unipolar p-type with no or only a small n-branch using either of the gates due to the large SBs for electrons in Pd-CNT contacts. Therefore the application of a negative back gate voltage (V_{BG}) switches the device off independent of the voltage applied to the CNT gate (V_{CNTG}) which shows that the field from the CNT gate does not influence the contact regions. In contrast, a device with a channel CNT which has a small, curvature induced band gap displays an ambipolar transfer characteristic when sweeping the back gate due to the small SBs for both holes and electrons (figure 5.5b). This enables us to create either p or n-type characteristics in the same device by changing the voltage on the back gate to either electrostatically p-dope the contact regions at negative V_{BG} or n-dope them at positive V_{BG}. This results in either p–i–p or n–i–n doping profiles in the semiconducting CNT where the doping in the intrinsic middle region is controlled by the voltage on the CNT gate (figure 5.5b).

The results from the simulations agree well with the measured transfer characteristics, however the off state can not be accurately modeled since only holes are taken into account and the method is unstable when calculating currents below 1 nA. The only fitting parameter parameter used in the simulations is the phonon scattering time τ_0 in eq. 5.7 and the SB height. The results from the experiments and simulations agree well for $\tau_0 = 0.13$ ps which is a few times lower than what was obtained by Zhou et al. [67]. The simulations show that the CNT gate modulates the carrier concentration

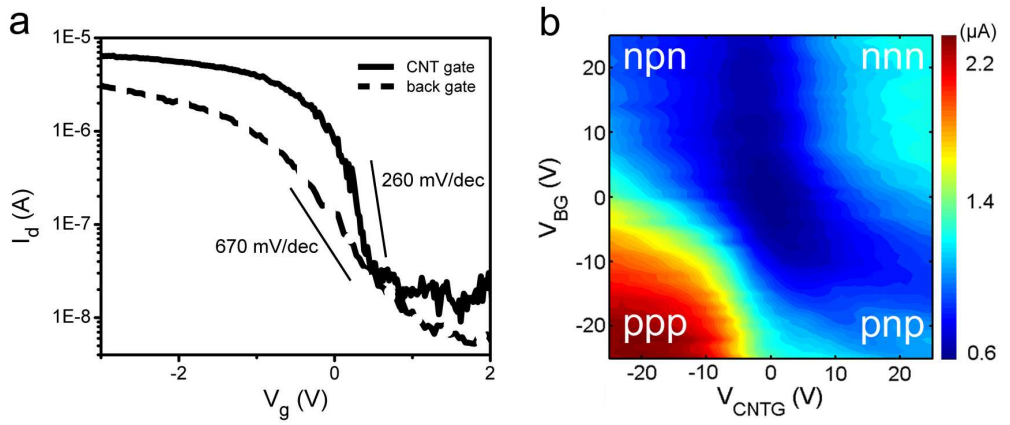

Figure 5.5: *a) Transfer characteristics of a CNT gated CNTFET obtained by sweeping the back gate with $V_{CNTG} = -5$ V or the CNT gate with $V_{BG} = -10$ V at $V_d = 1$ V. b) Contour plot of I_d as a function of both V_{CNTG} and V_{BG} at $V_d = 100$ mV for a another device with a small gap CNT as channel. The doping profiles along the semiconducting CNT at different gate voltages are indicated.*

locally but the length of the central region where the carrier concentration in the off state is reduced below half of that in the electrostatically doped contact regions is around 170 nm. This depleted region can be considered to be an approximate electrostatic gate length which is much longer than the physical gate length of 1.8 nm defined by the diameter of the gate CNT. In an electrostatically well behaved transistor, the gate length should be a few times larger than the screening length λ of the device since the potential in the channel is otherwise strongly influenced by the potentials in the source and drain resulting in short channel effects manifested by e.g. an increased inverse subthreshold slope [68]. λ increases with the thickness of the gate dielectric, decreases with its dielectric constant and is also dependent on the geometry e.g. whether it is a planar or coaxial gate. This restriction on the gate length is one of the major limiting factors when shrinking device dimensions since the thickness of the gate oxide has to be decreased with decreasing gate length to maintain good electrostatics which leads to increased gate leakage currents and high power consumption. For a CNTFET with a planar gate $\lambda = \sqrt{d_{CNT} d_{ox} \epsilon_{CNT} / \epsilon_{ox}}$, where ϵ_{CNT}, ϵ_{ox}, d_{CNT} and d_{ox} are the dielectric constants and diameters of the semiconducting CNT and the gate dielectric [68]. This means that for a CNTFET with 30 nm Si_3N_4 as the gate dielectric, the physical gate length should be longer than $\lambda = 10$ nm to avoid short channel effects [68]. However, since the segments of the semiconducting CNT that are electrostatically doped by the back

gate are so long, the potential in the source and drain contacts have little effect on the central region affected by the CNT gate. However, to more efficiently exploit the short physical gate length of the CNT gate, the gate dielectric needs to be considerably thinner or the dielectric constant higher which reduces the electrostatic gate length.

Even though the transfer characteristic of a transistor is measured using DC voltages it can still be used to predict its high frequency performance. The speed of a transistor can be described by the intrinsic gate delay

$$\tau = \frac{C_g V_{dd}}{I_{on}} \tag{5.9}$$

where C_g is the capacitance between the gate and channel, V_{dd} the power supply voltage used to switch the device between the on and off states and I_{on} the on state current. The gate delay describes how fast the charge $Q = C_g V_{dd}$ added to the channel by changing the gate voltage by V_{dd} is removed when the current I_{on} flows through the transistor and thus it gives a measure of the time needed to switch the device between the on and off states while τ^{-1} gives a measure of the intrinsic frequency limit of the device [3]. The gate delay decreases with gate length since less charge has to be moved during switching, which is one of the main reasons for scaling transistor dimensions. It should be noted that the intrinsic speed of a device is the maximum frequency that can be obtained in an ideal case, however in practice, parasitic capacitances between the gate, source and drain electrodes and interconnects degrade the performance considerably. In the CNT gated CNTFET, the large back gate is the main limitation to the high frequency performance and should therefore be replaced by local gates or through chemical doping of the segments close to the contacts as an alternative to electrostatic gating [123].

The gate capacitance in eq. 5.9 is extracted from the numerical simulations through $C_g = dQ/dV_g$ where Q is the charge on the semiconducting CNT. The calculated capacitances between the semiconducting CNT and the back gate and CNT gate are $C_{BG} = 15$ aF and $C_{CNT} = 10$ aF respectively. An analytical estimate of the capacitance to the back gate can be obtained by considering a cylinder with diameter d and length L separated from an infinite metallic plane by a dielectric with relative permittivity ϵ_r and thickness t_{di} which gives

$$C_{BG} = \frac{2\pi\epsilon_0\epsilon_r}{\cosh^{-1}(2t_{di}/d)} L \approx \frac{2\pi\epsilon_0\epsilon_r}{\ln(4t_{di}/d)} L. \tag{5.10}$$

For our device geometry eq. 5.10 gives a capacitance seven times higher than that obtained from the numerical simulations. This large discrepancy is most likely because our device has a quite small ratio between CNT length and dielectric thickness of only $L/h = 1.5$ which makes the analytical solution inaccurate. In addition to the pure geometrical capacitance there is also a contribution from the quantum capacitance, which is an intrinsic property of the semiconducting CNT which depends on its DOS [139]. However, since the quantum capacitance of CNTs of 4 pF/cm [140] is much larger than the geometrical capacitance it has little impact in our devices.

To use the gate delay metric for a fair comparison between different devices their I_{on}/I_{off} ratios have to be considered as well. The on and off states for a p-type transistor are usually defined at $V_{th} - 2/3V_{dd}$ and $V_{th} + 1/3V_{dd}$ respectively where V_{th} is the threshold voltage defined as the gate voltage at which the transconductance reaches its maximum (figure 5.6a)[1]. Compared to Si

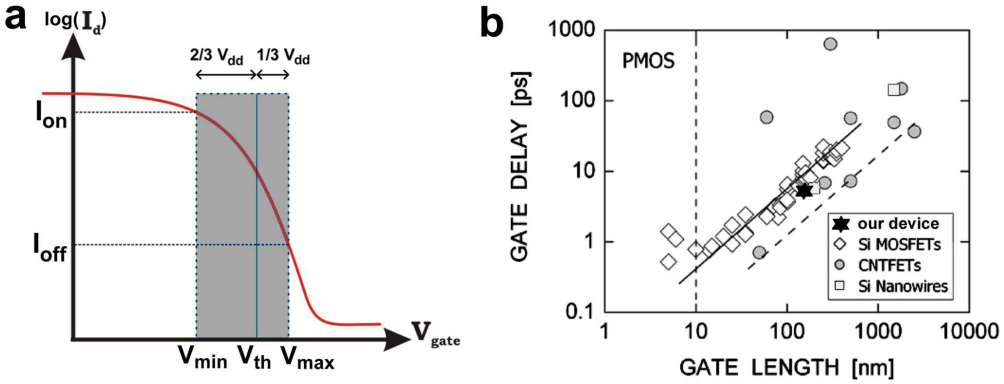

Figure 5.6: *a) Illustration of the definition of the on and off states in the transfer characteristic of a transistor used in the calculation of the gate delay and the on/off ratio. b) Gate delay as a function of gate length for p-type CNTFETs, Si MOSFETs, Si nanowire FETs and our CNT gated CNTFET. Adapted from [141].*

MOSFETs the V_{th} is poorly controlled in CNTFETs due to charge trapping as discussed previously so instead of determining V_{th} for our devices we move a window of width V_{dd} along the gate voltage axis and determine

[1] In many publications on CNTFETs, the on/off ratio refers to the maximum current ratio within a large gate voltage range. Even though this definition can be used to make a rough comparison between devices, it is not relevant for applications since for these the gate voltage is only varied within a limited range of $V_{dd} \approx 1\ V$.

the I_{on}, I_{off} and τ at each point. The maximum on/off ratio for our device using the CNT gate is 100 at which $\tau = 5$ ps.

The gate delay and on/off ratio is close to what is achieved in Ge/Si nanowires with gate lengths close to our electrostatic gate length [142], however the performance is still far from what is required for high performance logic applications [3]. Reducing V_{dd} gives a smaller τ but at the cost of reducing the on/off ratio. To enable a fair comparison with other devices $V_{dd} = V_d = 1$ V has been used in the calculations which is the power supply voltage presently used in commercial MOSFETs for logic computation. A comparison between the gate delays for Si MOSFETs, Si nanowire FETs and other CNTFETs with different channel lengths is shown in figure 5.6b. There is a large spread in the gate delays for CNTFETs most likely because the data is taken from different sources and the accuracies in using the analytical estimate of the capacitance in eq. 5.10 differ. In addition, the on/off ratios are typically lower for the CNTFET devices compared to the Si MOSFETs. If the electrostatic gate length is used for the comparison, the gate delay for the CNT gated CNTFET is close to what is achieved in Si MOSFET with similar gate lengths. On the other hand, if the physical gate length is used instead, the gate delay is considerably higher compared to the corresponding Si MOSFETs.

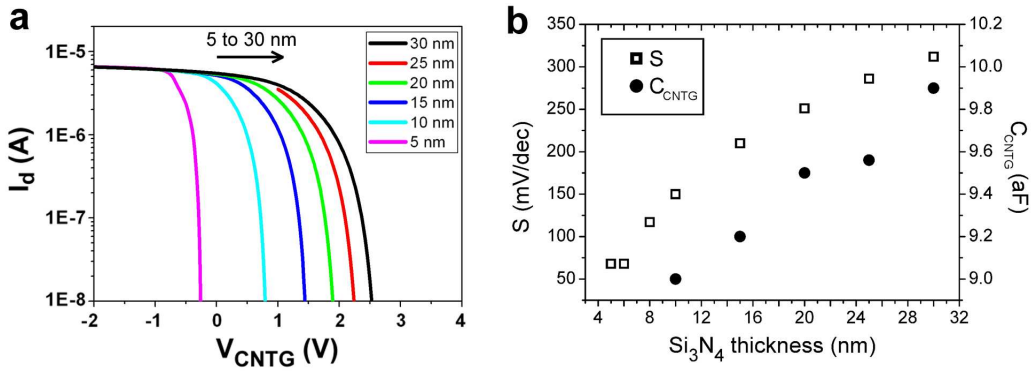

Figure 5.7: *a) Simulated transfer characteristics using the CNT gate with $V_d = 1$ V for devices with 5 to 30 nm (left to right) Si_3N_4 dielectric thickness. b) Inverse subthreshold slope and CNT gate capacitance as a function of Si_3N_4 thickness.*

The thickness of the Si_3N_4 dielectric has been varied in the simulations to study whether the device performance can be improved. The calculated transfer characteristics illustrate that the inverse subthreshold slope and therefore also the gate delay is decreased with decreasing dielectric thickness

(figure 5.7). The calculations also show that the capacitance to the CNT gate does not change considerably as the dielectric thickness is decreased. However, since the effective gate length is reduced, the capacitance per unit length in the region affected by the CNT gate is increased with reduced Si_3N_4 thickness. Therefore, reducing the gate dielectric thickness improves the gate coupling and consequently decreases the inverse subthreshold slope. For a 5 nm thick dielectric the inverse subthreshold slope $S = 70$ mV/dec resulting in a delay time $\tau = 1.4$ ps which corresponds to an intrinsic frequency of 700 GHz.

5.5 CNTFETs with suspended CNT gates

Even though the simulations show that the inverse subthreshold slope can be improved by reducing the thickness of the gate dielectric it is still limited to 60 mV/dec at room temperature even for very thin dielectrics. To obtain an inverse subthreshold slope lower than the thermal limit, the development of a CNTFET with a suspended CNT gate, where the gate dielectric has been replaced by an air gap, is being pursued (figure 5.8a).

It has been demonstrated that an inverse subthreshold slope of 2 mV/dec can be achieved in Si MOSFETs with a suspended gate due to the abrupt change in capacitance as the gate is pulled in towards the gate oxide [143]. However, the operation of such device relies on the gate snapping into contact with the surface and thus large hysteresis is present in the transfer characteristic due to the large change in gate voltage needed to release the gate electrode. In our device design, the CNT gate should not snap into contact with the surface but instead stay suspended during operation. As in a device with a non-suspended gate, a fixed negative voltage applied to the back gate is used to electrostatically dope the semiconducting CNT with holes. Likewise, the suspended CNT gate is used to induce a local potential barrier, but in addition the mechanical motion of the CNT gate is exploited to obtain a small inverse subthreshold slope. If the voltage difference V_{CNTG} between the suspended CNT gate and the semiconducting CNT is changed by ΔV_{CNTG} there will be an additional attractive electrostatic force

$$F_{elec} = \frac{1}{2} C'_{CNTG} \Delta V_{CNTG}^2 + C'_{CNTG} V_{CNTG} \Delta V_{CNTG} \tag{5.11}$$

where $C'_{CNTG} = dC_{CNTG}/dz$ is the gradient of the capacitance with respect to the distance between the the two CNTs. The electrostatic force causes

the gate CNT to bend down which changes the capacitance between the CNTs by ΔC_{CNTG} resulting in a change of the charge on the semiconducting CNT

$$\Delta Q = \Delta(C_{CNTG}V_{CNTG}) = C_{CNTG}\Delta V_{CNTG} + \Delta C_{CNTG}V_{CNTG} \qquad (5.12)$$

where the first term on the right hand side corresponds to the charge induced by the electrostatic gating effect and the second term the charge induced by the mechanical motion [11]. Since the conductance of the semiconducting CNT depends on the induced charge, the mechanical motion results in a more rapid change in current with respect to gate voltage compared to a device with a static gate [67].

Numerical simulations of a device with a suspended CNT gate where it is either kept at a fixed distance from the semiconducting CNT or allowed to move asserts that a device with a moving CNT gate has a significantly improved transfer characteristic compared to one with a static gate (figure 5.8b). The simulations show that for a device with 30 nm distance

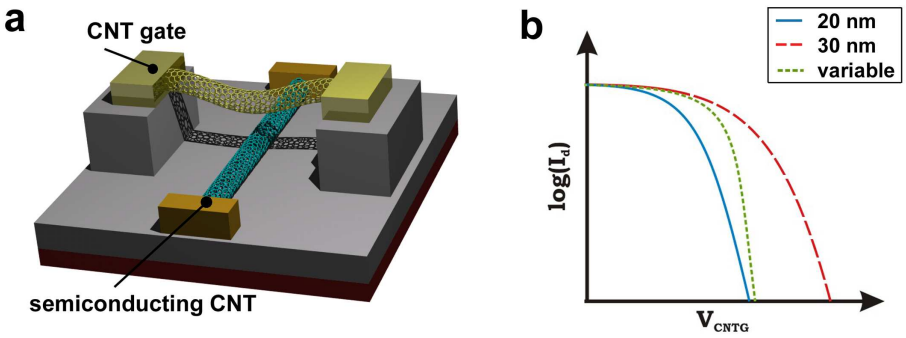

Figure 5.8: *a) Schematic of CNTFET with a suspended CNT gate. b) Schematic transfer characteristics with 20 nm, 30 nm and variable spacing between the gate and semiconducting CNTs.*

between the CNTs and a length of the gate CNT of 2 µm , the inverse subthreshold slope is only 32 mV/dec which is half of the thermal limit for a device with a non-suspended gate [144]. Not only has the device good transistor characteristics but the semiconducting bottom CNT can also be used to detect the deflection of the CNT with a maximum sensitivity of $\partial I_d/\partial z = 1.7$ µA /nm, a feature which can be used for sensitive displacement sensing [145].

The small device dimensions proposed in the theoretical model in [144] are however challenging to realise experimentally. The device fabrication faces

difficulties such as poor control of the distance between the CNTs due to uncontrolled amount of slack in the gate CNT making it difficult to reproducibly fabricate devices with a small gap. Devices with suspended CNTs have previously been fabricated by clamping the CNTs with electrodes and subsequently removing the underlying SiO_2 through wet etching, however this requires large trench depths and critical point drying to avoid that the CNTs fall down and stick to the substrate during processing [146]. It is also challenging to use this method for devices with crossed CNTs since the etching has to be precisely controlled to avoid shifting the position of the lower CNT. Instead, a two step growth method similar to the one used for devices with non-suspended CNT gates has been used. The CNTs from the first CVD step are located and Ti/Mo side electrodes and source and drain contacts are patterned. New catalyst is patterned on the edges of the side electrodes and a second CVD step is used to grow the gate CNTs. Many of the devices have suspended CNTs between the side electrodes but usually there are also non-suspended CNTs that short circuit the side electrodes to the lower CNT (figure 5.9). Since only some of the CNTs grown in the second step are suspended, the yield of good devices is low and improvements are needed in the design and fabrication methods of the devices.

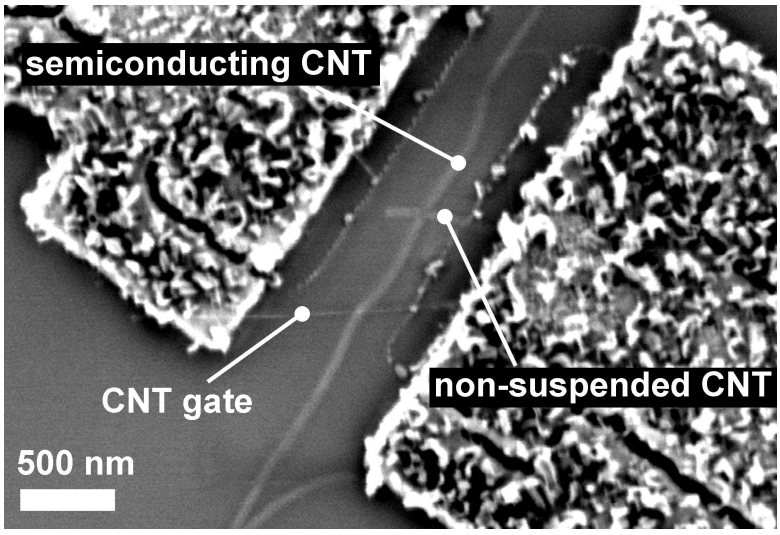

Figure 5.9: *SEM image of a CNTFET with a suspended CNT gate. In addition to a gate CNT suspended between the side electrodes, there are also CNTs on the substrate that short circuits the channel and gate CNTs.*

5.6 Conclusions

The CNT gated CNTFET device presented in this chapter should be viewed as a proof-of-principle that CNTs can function both as channels and gate electrodes taking benefit of the excellent electrical properties of both semiconducting and metallic CNTs. The fabrication method using two CVD steps allows for the fabrication of all-CNT based FETs with gate delay times competitive with Si MOSFETs and that show promise of improved performance with decreased dielectric thickness. Since the effective mass of the charge carriers is low in CNTs, and the gradient of the potential is large in the region between the segments doped by the back gate and the CNT gate, carriers can tunnel between the bands if the maximum of the valence band in the contact regions has a higher energy than the minimum of the conduction band in the CNT gated region in a p-i-p doped device. Such band-to-band tunneling can be exploited to produce devices with an inverse subthreshold slope lower than the thermionic limit but for devices with small band gap CNTs it sets an upper limit on the lowest off state current that can be achieved [147].

In spite of the good DC performance there are still many improvements that have to be done to make these devices competitive for high frequency logic computation. The high frequency performance of the CNT gated CNTFETs is limited by the parasitic capacitances to the back gate which should ideally be replaced by local gates or chemical doping of the semiconducting CNT. Even though it is possible to optimise the device design for high frequency applications, the need for higher reproducibility during fabrication still has to be solved. The methods used give a yield which is inadequate for large scale integration due to the lack of control of the positions of the CNTs and the devices also display differences in performance intolerable for many applications. There is also no selectivity in the growth resulting in a mixture of metallic and semiconducting CNTs which contributes to the poor yield. Since the second growth step is performed without an applied electric field there is no directional control but the introduction of different positioning techniques that can be used for both the channel and the gate CNTs, such as alignment by crystallographic steps [148] or by the direction of the gas flow during CVD [149], should hopefully increase the yield and therefore enable large scale production of CNT gated CNTFETs.

Chapter 6

Schottky barriers in CNT-metal contacts

In contrast to conventional Si MOSFETs that use source and drain contacts that are oppositely doped compared to the channel, CNTFETs usually have metal contacts. For most contacts between a metal and a CNT, a Schottky barrier (SB) forms at the junction. For transistor applications, a low SB for either holes or electrons is preferable since that not only reduces the contact resistance but also results in a good on/off ratio and a small inverse subthreshold slope. In contrast, in Schottky diodes suitable for high frequency applications such as detectors, mixers, and frequency multipliers a large SB at one contact and a negligible SB at the other is required for good current rectification [8, 150]. Therefore, to properly design different CNT devices it is important to gain an understanding of how SBs in CNT-metal contacts are formed and what factors influence their heights.

In this chapter, an introduction to the formation and transport physics of SBs is given with emphasis on CNT-metal contacts. A more in depth discussion of the physics of metal-semiconductor contacts can be found in [151] and in [152]. The results from a study of the impact of CNT diameter on the SB height in Pd-CNT contacts presented in paper VI are also discussed. Further, preliminary results from measurements of SB heights in devices that have different metals as contacts to CNTs are presented.

6.1 Schottky barrier formation

If a metal and a semiconductor are joined and the Fermi level in the semiconductor is higher in energy than that in the metal, electrons move from the semiconductor into the metal leaving a positive background of ionised atoms. Electrons continue to be transported across the interface until the Fermi levels of the two systems have equilibrated (figure 6.1). A SB for holes (electrons) arises due to the mismatch between the Fermi level of the metal and the valence (conduction) band of the semiconductor. According to the first theoretical descriptions of metal-semiconductor contacts by Schottky [153] and Mott [154], the SB height for electrons is

$$\Phi_{SBe} = \phi_m - \chi \tag{6.1}$$

where ϕ_m is the work function of the metal which is the energy needed to remove an electron from the Fermi level into vacuum and χ the electron affinity of the semiconductor which is the energy needed to remove an electron from the bottom of the conduction band. Consequently, the barrier height for holes is given by $\Phi_{SBh} = \chi + E_g - \phi_m = I_s - \Phi_m$ where E_g is the band gap and I_s the ionisation potential of the semiconductor which corresponds to the energy difference between the top of the valence band and vacuum.

However, it has been observed that for many semiconductors, the SB height is almost independent on what metal is chosen for the contact. Thus, the SB height do not follow the simple relation in eq. 6.1 but instead have a much weaker dependence on the metal work function, a phenomenon known as Fermi level pinning. This weak dependence has been attributed to interface states with energies within the band gap of the semiconductor that are present in close vicinity of the metal (figure 6.1c). It is possible to define a charge neutrality level Φ_0 for the interface states measured from the top of the valence band. States lower in energy than Φ_0 are of donor type and positively charged when empty and states higher in energy than Φ_0 are of acceptor type and negatively charged when full. This means that if the Fermi level of the semiconductor coincides with Φ_0, there is no charge trapped in the interface states but if it is above or below Φ_0 the surface has a negative or positive charge Q_{ss} respectively. This charge, together with any space charge in the depletion layer, is balanced by an equal amount of charge of opposite sign on the metal surface which results in a dipole over a distance δ of atomic dimensions. The potential drop over this dipole modifies the SB height from the Shottky-Mott relation in eq. 6.1. Therefore

in the presence of interface states, the SB height for electrons can instead be described by

$$\Phi_{SBe} = \gamma(\Phi_m - \chi) + (1 - \gamma)(E_g - \Phi_0) \tag{6.2}$$

where

$$\gamma = \frac{1}{1 + \frac{qD_{it}\delta}{\epsilon_i}} \tag{6.3}$$

where ϵ_i is the permittivity of the interface and D_{it} the density of interface states [155]. If D_{it} is large, $\gamma \to 0$ which means that the SB height approaches $\Phi_{SBe} = E_g - \Phi_0$ and is determined entirely by the interface states and is completely independent of metal work function while in the absence of interface states, $\gamma \to 1$ and the Schottky–Mott limit described by eq. 6.1 is obtained. The variation of the SB height as a function of the metal work function for different metal contacts on a certain semiconductor gives a measure of the strength of the Fermi level pinning and can in principle be used to estimate D_{it}.

There are several different theories that attribute the occurrence of interface states to different mechanisms. The metal induced gap states (MIGS) theory states that the wavefunctions of the electrons in the metal have tails extending a few Å into the surface of the semiconductor that give rise to interface states in the band gap [156]. Another theory attributes the interface states to the creation of defects in the semiconductor as the metal is deposited on the surface [157]. More recently, the chemical bond polarisation theory was developed to explain the discrepancy of measured SBs in metal-semiconductor contacts that have different crystallographic structure but the same materials [158]. According to this theory, the most significant effect that gives rise to the dipole that alters the SB height from the Schottky-Mott limit is the charge rearrangement that occurs when bonds are formed and not interface states. The chemical bond polarisation theory gives a similar description of the SB height as eq. 6.2 but where γ depends on the density of bonds instead of the density of interface states.

Due to Fermi level pinning, it is difficult to predict the behaviour of a certain metal-semiconductor combination from the properties of the separate materials, something which is desirable for many applications. Successful attempts to control the SB include passivation of the semiconductor surface by different elements to remove dangling bonds prior to metal deposition [160], introducing polar molecules at the interface [161] and putting a high concentration of dopants close to the interface which does not alter the

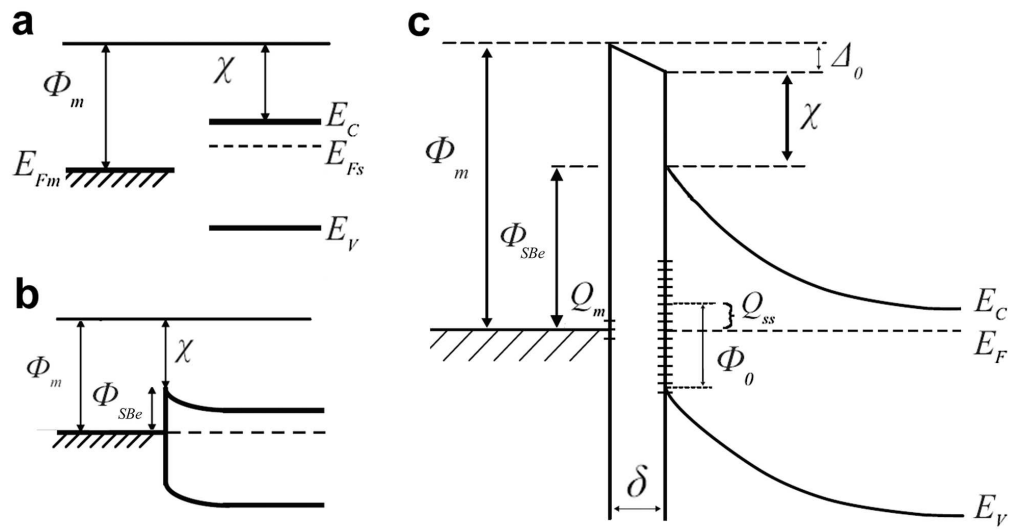

Figure 6.1: *a) Energy band diagram before contact is made between a metal and a n-type semiconductor. b) When contact is made, the Fermi levels equilibrate and a SB arise. The image depicts a case without interface states. c) Energy band diagram of a contact between a metal and a n-type semiconductor with interface states in the band gap at the semiconductor surface. The charge Q_{ss} in the interface states create a dipole over a distance δ that lowers the barrier height by Δ_0. The notations used are defined in the main text. Adapted from [159].*

height but makes the SB thin enough to result in a significant tunneling current [162]. It should also be noted that the tabulated values of metal work functions and electron affinities of semiconductors correspond to free surfaces and thus can not reliably be used in eq. 6.2. In a metal-semiconductor contact both of these are altered from the values corresponding to a free surface due to relaxation and reconstruction of bonds. The metal work function is also sensitive to the surface structure with differences of 100s of meV for different crystal orientations [163].

6.2 Theoretical modeling of CNT-metal contacts

The SBs between CNTs and different metals have been studied theoretically both by electrostatic modeling and by density functional theory (DFT) that calculates the charge density distribution on a microscopic scale. Some of

these studies, which often have contradicting conclusions, are reviewed in this chapter.

Léonard et al. [164] have considered a side contacted CNT and studied whether interface states affect the SB height by adding a sheet of charge around a CNT. As the density of the charge is increased, the SB height is shifted from its unperturbed initial value, however due to the competition with the large charge density in the van Hove singularities at the band edges in the CNT the added charge density has to be 100 times larger than in a bulk contact to induce any pinning (figure 6.2a).

In contrast to the side-bonded contacts described above, in an end-bonded geometry the metal is only connected to the tip of a CNT. For such geometry it has been predicted that the influence of pinning is much lower than for a planar contact between two bulk materials [165]. In contrast to a planar junction, where a dipole sheet created by interface states shifts the energies of the bands relative to the metal Fermi level very deep into in the semiconductor, the dipole in an end-bonded geometry is localised and thus its potential decays rapidly within the semiconductor (figure 6.2b). Therefore, the interface states shift the bands within a depth of only a few nanometers from the junction creating a thin tunneling barrier while the energies of the bands deeper into the CNT are the same as for a contact without interface states.

In contrast to most bulk metal-semiconductor junctions, these two studies predict that the SB height should be fully controlled by the metal work function in a CNT-metal contact and its height given by the Schottky-Mott relation in eq. 6.1 (figure 6.3b). Since the band gap of a CNT $E_g \propto 1/d$ the SB heights for both holes and electrons are expected to be inversely proportional to the diameter (figure 6.3a).

However, the proportionality constants between CNT diameter and band gap reported in the literature vary between 0.71 and 0.93 $\mathrm{eV} \cdot \mathrm{nm}$ [42, 164, 168] while experimentally measured work functions of CNTs vary between 4.8 and 5.05 eV [169–171]. This means that for a Pd contact to a CNT with a diameter of 1 nm, the SB height for holes is be predicted to be in the range 35-406 meV depending on what values are chosen from the literature. It has also been theoretically predicted that not only the diameter but the exact chirality has a large impact on both work functions and band gaps, and therefore also the Schottky barriers, of CNTs with diameter smaller than 0.8 nm [172]. Thus, even if CNT-metal contacts are not influenced by

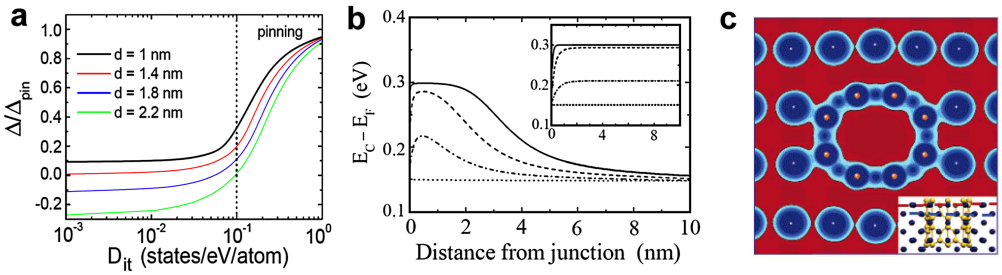

Figure 6.2: *Results from three different theoretical studies of CNT-metal contacts. a) SB height as a function of the density of interface states for CNTs with different diameters in a side-bonded configuration. The dashed lines indicate the onset of pinning. The pinned height of the SB is* $\Delta_{pin} = E_g/2$. *Adapted from [164]. b) Conduction band minimum as a function of distance from an end bonded CNT-metal junction at different density of interface states. The inset shows the corresponding result for a planar junction. Adapted from [165]. c) Contour plot of the electrostatic potential for a (8,0) CNT embedded in Pd atoms calculated using density functional theory. The main image shows the cross section indicated by the red line in the inset. The overlapping potentials between four Pd atoms and neighbouring carbon atoms illustrate the absence of a potential barrier. Adapted from [166].*

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interface states, it is difficult to design a device with a predetermined SB height.

In contrast to the electrostatic simulations discussed previously, DFT calculations on CNT-metal contacts only consider small diameter CNTs and the metals are limited to a few atomic planes due to the large computational resources required (figure 6.2c). Some results obtained by DFT calculations suggest that the DOS of a CNT becomes severely distorted when contacted by Ti or Pd and its band gap filled with interface states [166, 173]. This implies that any SB present would be between a metallic like and semiconducting part of the same CNT instead of between the metal contact and the CNT. According to [174], a ring of Pd atoms surrounding a CNT give a SB height of 0.4 eV for holes between a metal covered and an exposed part of a (8,0) CNT. A variable amount of such "metal-poisoning" has also been taken into account in models that have been used to calculate the transfer characteristics of CNTFETs [68, 167].

A few different contact metals have been studied using DFT and it has been found that Al and Au form fewer bonds to CNTs compared to Pd [175, 176].

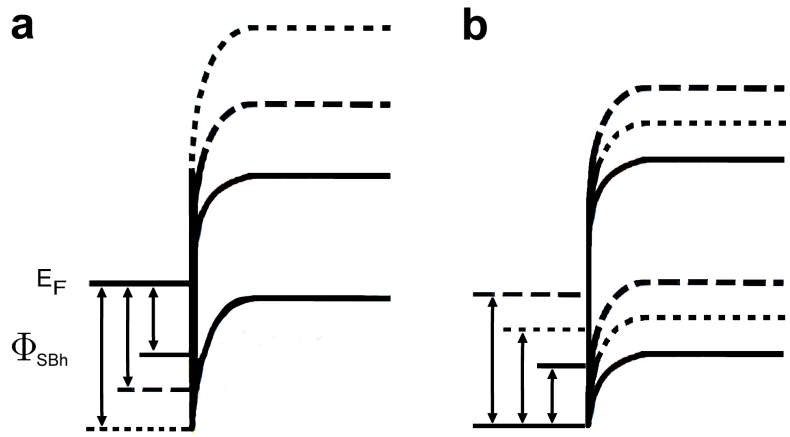

Figure 6.3: *Schematic band diagrams of the contacts between metals and p-doped CNTs in the absence of Fermi level pinning. The arrows indicate the distance between the Fermi level of the metal and the top of the valence band in the CNT at the interface which corresponds to the SB height for holes. To simplify, the same distance is used between the top of the valence band and the Fermi level for all CNTs. a) Contacts to CNTs with large (solid line), intermediate (dashed line) and small (dotted line) diameters. The CNT with the largest diameter has the smallest band gap and thus the lowest SB. b) Contacts using metals with high (solid line), intermediate (dotted line) and low (dashed line) work functions. The metal with the highest work function gives the lowest SB for holes. Adapted from [167].*

A comparison between Au and Pd which have similar work functions illustrate that Pd forms a more transparent contact than Au due to the strong electronic coupling to the CNT [175]. In addition, the crystallographic structure of the metal surface is of importance with up to 0.2 eV difference in SB height between different orientations [177]. The contact geometry is also important and it has been concluded that a junction where Al is bonded to the end of a CNT has a considerably higher SB compared to a side bonded configuration [176].

The SB heights between CNTs and Pd, Al and Sc contacts have also been calculated using chemical bond polarisation theory [178]. The calculation shows that due to the different electronegativity of carbon and the contact metals there is a charge redistribution in the bonds and a dipole induced at the contact which alters the SB from the ideal Schottky-Mott limit.

In contrast to the results from electrostatic modeling [164, 165] most DFT

calculations indicate that the microscopic properties such as crystal orientation, bond configuration, presence of interface states in the band gap and bond polarisation have a large impact on the SB heights for CNT-metal contacts. However, it is very difficult to experimentally study or control the contact on a microscopic level since the evaporated metals consist of grains with a variety of crystal orientations and there can also be oxide layers or contaminations from for example resist residues present at the CNT-metal interface.

6.3 Current transport in Schottky barriers

The main transport mechanisms in a metal-semiconductor contact are thermionic emission over the SB, tunneling through the SB and recombination and generation in the space-charge region and in the neutral region (figure 6.4a). Thermionic emission can occur when an electron has sufficient energy to pass over the SB resulting in a current consisting of only the highest energy electrons from the metal or the semiconductor. However, electrons moving from the semiconductor into the metal have to pass through the depletion layer before they transverse the SB. If the mean free path of electrons is small, the transport through the depletion layer can be considered to be in series with the thermionic emission process. However, most semiconductors have a mobility which is high enough so that thermionic emission is the main current limitation and drift-diffusion within the depletion layer can be ignored [151].

If thermionic emission is the only transport mechanism in a SB, the electron current from the semiconductor to the metal increases exponentially with voltage at a forward bias but saturates at reverse bias since the barrier for thermionic emission from the metal to the semiconductor is unchanged. However, additional current contributions from tunneling and barrier lowering effects are usually also present. Classically, electrons can only pass over a SB but quantum mechanical tunneling allow also electrons with lower energies to pass through SB. A significant amount of tunneling is only possible if a SB is sufficiently thin since the tunneling probability is quickly reduced with increasing barrier thickness. The barrier thickness can be reduced by increasing the electric field close to the interface by e.g. increasing the doping of the semiconductor. The tunneling current is also larger in a reversed biased compared to a forward biased SB due to the thinner barrier and has

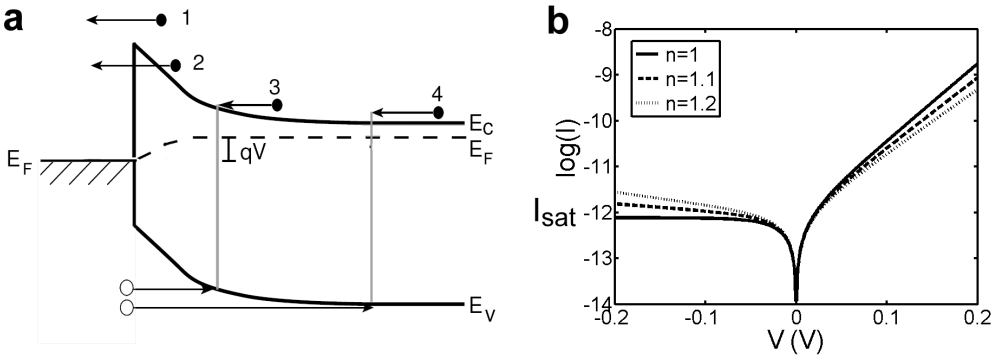

Figure 6.4: *a) Transport in a metal contact to a n-type semiconductor at a forward bias V. 1) Thermionic emission over the SB. 2) Tunneling through the SB. 3) Recombination in the depletion region. 4) Recombination in the neutral region. b) IV characteristic of a metal-semiconductor contact obtained using the ideal diode equation (eq. 6.4) with different ideality factors.*

a weaker temperature dependence compared to thermionic emission which means that it dominates transport at low temperatures [179].

In contrast to bulk semiconductors, high doping levels are not needed in CNTFETs to achieve a considerable amount of tunneling. This is due to the small diameters of the CNTs that give electrostatics that lead to focusing of the electric field from the gate at the contacts [59]. For thin gate oxides and electrodes, the strong field at the contacts makes the SBs thin enough to allow significant tunneling compared to thicker oxides.

In addition to tunneling there are mainly two mechanisms that can increase the current through a SB as the reverse voltage across a junction is increased. The SB height can be modified by image force lowering which is due to than an electron passing the barrier into the semiconductor leave a positive mirror charge in the metal. The electrostatic attraction between the electron and its mirror image cause the barrier to be lowered. The image force barrier lowering is proportional to $V^{1/4}$ where V is the reverse voltage applied to the semiconductor. In addition to image force lowering the SB height can also be modified by a potential drop over any interfacial layer present at the junction. This gives rise to a SB lowering proportional to $V^{1/2}$.

The electron current due to thermionic emission in a SB between two bulk

materials is given by the ideal diode equation

$$I = \overbrace{AA^*T^2 e^{-\frac{q\Phi_{SBe}}{k_B T}}}^{I_{sat}} e^{\frac{qV}{nk_B T}} \left(1 - e^{-\frac{qV}{k_B T}}\right) \tag{6.4}$$

where A is the contact area, $A^* = 4\pi m^* q k_B^2/h^3$ the effective Richardson's constant where m^* is the effective mass, V the voltage applied to the semiconductor, T the temperature, n the ideality factor and I_{sat} the saturation current [151]. A generalisation of eq. 6.4 for N-dimensional materials gives a temperature dependence of $T^{(N+1)/2}$ and a Richardson's constant of $A^* = 2^{(N+1)/2}\pi^{(N-1)/2} m^{*(N-1)/2} q k_B^{(N+1)/2} h^{-N}$ due to the different DOS in different dimensions [180]. The ideality factor $n = (1 - \partial\Phi_{SBe}/\partial V)^{-1}$ which describes the dependence of the barrier height on the applied voltage includes barrier lowering effects such as image force lowering, and voltage drops over interfacial layers as well as tunneling. In the ideal case with $n = 1$ there are no mechanisms that lowers the barrier and the current saturates at I_{sat} for a reverse bias larger than a few times $k_B T$ since the reverse thermionic emission current injected into the metal from the semiconductor (first term in the parenthesis in eq. 6.4) vanishes. However, if $n > 1$ the current in the reverse direction increases exponentially with bias while the current for a forward bias is lowered compared to the ideal case (figure 6.4b). If $n > 1.2$ the current is not dominated by thermionic emission and eq. 6.4 can not be used reliably.

For bulk metal-semiconductor contacts there are several methods to measure the SB height. If transport is dominated by thermionic emission and the contact area and the effective Richardson's constant are known, an estimate of an effective SB height at zero bias can be obtained directly from the IV characteristic by extrapolating a plot of $ln(I/(1 - e^{-qV/k_B T}))$ as a function of applied voltage to $V = 0$ V. However the electrically active area is difficult to estimate since it may differ considerably from the geometrical area of the contact due to e.g. diffusion between the materials.

Since the saturation current in eq. 6.4 can be rewritten as

$$log\left(\frac{I_{sat}}{T^2}\right) = log(AA^*) - \frac{q\Phi_{SBe}}{k_B T}, \tag{6.5}$$

measuring the IV characteristic for different temperatures and plotting $log(I_{sat}/T^2)$ as a function of 1/T in an Arrhenius plot gives a slope of

$-q\Phi_{SBe}/k_B$ and an intersection with the y-axis equal to $log(AA^*)$. This activation energy method is beneficial since it alleviates the need of knowing the effective Richardson's constant and the area to extract the SB height.

SB heights can also be extracted from CV measurements since the depletion region in a SB is acting as a parallel-plate capacitor with a decrease in capacitance with increasing reverse bias due to the increase of the depletion width. However, the CV method can not be used for small barriers due to the large current at reverse bias and is difficult to implement for measurements of SBs in CNT-metal contacts due to the small capacitances between the CNTs and the electrodes. Another method to measure SB heights is to exploit the photoelectric effect by measuring the photon energy needed to generate a current through metal-semiconductor contacts as they are illuminated.

6.4 Experimental studies of CNT-metal contacts

For CNTFETs, a low SB height for either holes or electrons is preferable depending on if a p or n-type device is desired. A low SB enables a high on current and a low off current which is crucial for logic applications. In addition, for a CNTFET with non-zero SB heights and a thin gate dielectric, an inverse subthreshold slope close to the thermal limit of 60 mV/dec can not be achieved since it is tunneling and not thermionic emission that limits the current [60]. It has been shown that Pd contacts to CNTs with diameter larger than 1.6 nm give ohmic p-type characteristics with high on-currents which has been attributed to the high work function of Pd [51]. After the devices were exposed to hydrogen, the on-current decreased and the transfer characteristic became more ambipolar due to lowering of the Pd work function. However, the metal work function is not the sole factor that determines the on-state current but the adhesion between the CNT and the metal is also important since a tunneling barrier that limits the current may form in series with a SB [181]. Au and Pt which have work functions similar to Pd give lower on-currents which have been attributed to weaker adhesion to the CNTs [182, 183]. Nosho et al. used Pd, Ti, Mg and Ca to contact CNTs and observed an increase in the on-state current of the hole branch of the transfer characteristic with increasing metal work function [184]. Most low work function metals oxidise easily and it is therefore difficult to obtain n-type CNTFETs that have stable electrical properties in air. The best

n-type CNTFETs fabricated without doping use Sc or Y as contact metals resulting in stable devices with high electron on-currents [61, 185].

For CNT-metal contacts it is not possible to extract the SB height directly from the IV characteristic since neither the contact area nor the Richardson's constant are known. Since the capacitance between the metal contact and the CNT is only 10s of aF it is challenging to directly use the CV method to extract the SB height. However, by combining measurements using a sensitive capacitance bridge with numerical calculations Tseng et al. obtained SB heights for CNTs contacted by Ti, Nb and Cr and concluded that the Fermi level is not pinned by interface states [186].

Another strategy which has previously been used is to measure the on-state currents of CNTFETs and use numerical simulations to relate them to a certain SB height [167]. The results suggest that the SB height is inversely proportional to the CNT diameter. However, it should be noted that in this study the diameters were not measured on the electrically characterised CNTFETs but instead derived from a statistical treatment of data from TEM images of the original CNT material. The authors also concluded that the SB heights are reduced with increasing metal work function for Pd, Ti and Al contacts but do not correspond to the values expected using the clean metal work functions.

The two methods described above require additional theoretical simulations to extract SB heights but except for such "indirect" measurements of SB heights there have previously only been measurements on single CNT devices. Appenzeller et al. used the activation energy method described in the previous section to extract the SB for a Ti contacted CNT [187]. The authors measured the transfer characteristic at five temperatures, and extracted an activation energy at different gate voltages from the slopes of the data plotted in Arrhenius plots. The activation energy was plotted as a function of gate voltage and the SB height extracted from the point when the slope of this curve was equal to one since this corresponds to flat band conditions at one of the contacts i.e. thermionic emission should dominate over tunneling. The authors also conclude that for thick gate dielectrics and large diameter CNTs, tunneling is negligible and the thermionic emission limit should be reached for all negative gate voltages. The authors find a SB height which is close to half the band gap of the CNT. However, the transfer characteristic of their device is p-type without any n-branch indicating that the SB height for holes is considerably lower than that for electrons. Any tunneling or thermionic emission of electrons at high gate voltages are also disregarded in their analysis.

A similar measurement approach was used by Chen et al. who studied a Cr contacted CNT [64]. After passing a high current through the CNT in vacuum, the device showed an ambipolar transfer characteristic. The transfer characteristic was measured at different temperatures and the resulting activation energy as a function of gate voltage showed a maximum corresponding to the SB height. It was concluded that the barrier is half the band gap which is expected using the Schottky-Mott theory for a Cr-CNT contact. The main difference in the procedure compared to the method used by Appenzeller et al. [187] is the position in the activation energy vs gate voltage plot where the SB height is extracted. The authors in [64] argue that for the thick gate dielectric used in their device, tunneling through the SBs should be negligible at small gate voltages and transport dominated by thermionic emission. However, if tunneling is negligible it is possible that the measured barrier is not only the SB height but has an additional barrier induced by the gate voltage due to the bending of the bands in the bulk of the CNT. According to Nosho et al. who used Ca as contact metal to create n-type CNTFETs, the activation energy extracted from temperature dependent measurements approaches the true SB height for decreasing gate voltage. However, for their unipolar device where only a n-branch is observable, the activation energy for large negative gate voltages would correspond to the SB height plus an additional gate induced barrier [188].

The depletion regions in CNT-metal contacts have been imaged using photocurrent and photovoltage measurements [189] as well as by scanned gate microscopy [190]. In the scanned gate microscopy experiments it was observed that a biased AFM tip scanned over a CNTFET has a stronger gating effect when the tip is in the vicinity of one of the contacts implying that a barrier is present there. The results from photovoltage measurements used to image the depletion region by irradiating the CNT-metal contact with a laser illustrates that the depletion width can extend up to 1.5 μm from the edge of the contact into the CNT at a gate voltage corresponding to the off-state of the device and decrease below 400 nm in the on-state. Even though a quantitative value of the SB height could not be deduced from this experiment but it was clear that the hole barrier is considerably higher than the electron barrier in a Pd contacted device. Interestingly, the photovoltage measurements show that the depletion width is not limited to the diameter of the CNT as is assumed in the theoretical description that predicts no effect of Fermi level pinning for side bonded CNTs [164] but instead can extend into the part of the CNT not covered by the contacts.

6.5 Schottky barrier height for CNTs with different diameter

To obtain a low SB height in a CNTFET, a large diameter CNT which has a small band gap is beneficial. However, a small band gap gives low barriers for both holes and electrons resulting in large off state leakage currents and a thus a poor on/off ratio. In contrast, a small diameter CNT gives a high on/off ratio but the higher SB reduce the on state current. Therefore, there is an optimum diameter where the SB height is low but the band gap is large enough to prevent large leakage currents in the off-state. This optimum diameter can be determined by measuring the SB height as a function of diameter for a number of devices. In this section the results presented in paper VI are summarised and discussed. For a more detailed description of the experiments and their results the reader is referred to the paper.

To study the dependence of the SB height on CNT diameter, Pd was chosen as the contact material due to its ability to form stable contacts to semiconducting CNTs. A detailed description of the fabrication of CNTFETs with Pd contacts can be found in appendix A. The transfer characteristics of the devices were measured in vacuum at different temperatures with the source contact grounded and a small bias of $V_d = 100$ mV applied to the drain (figure 6.5). The devices are equivalent to two Schottky diodes connected back-to-back, with the source forward biased and the drain reversed biased with respect to holes, with a series resistance corresponding to scattering in the bulk of the CNT in between (lower inset in figure 6.5a).

For large band gap semiconducting CNTs the off-state current increases exponentially with temperature while the on-state current at large negative gate voltages decreases (figure 6.5a). In the off-state, the SB at the drain contact is too wide to allow for considerable tunneling and the main resistance of the device is due to thermionic emission over it. However, at large negative gate voltages the barrier width is decreased considerably and tunneling dominates the transport reducing the contact resistance. The transport at these gate voltages is limited by the bulk resistance of the CNT instead of the contact resistance which means that the current has an opposite temperature dependence compared to the off state due to increased scattering at higher temperatures. The bulk resistance dominates the characteristic in CNTFETs with long CNTs [191] or low SBs [51]. The current through a small band gap CNT that displays an ambipolar characteristic

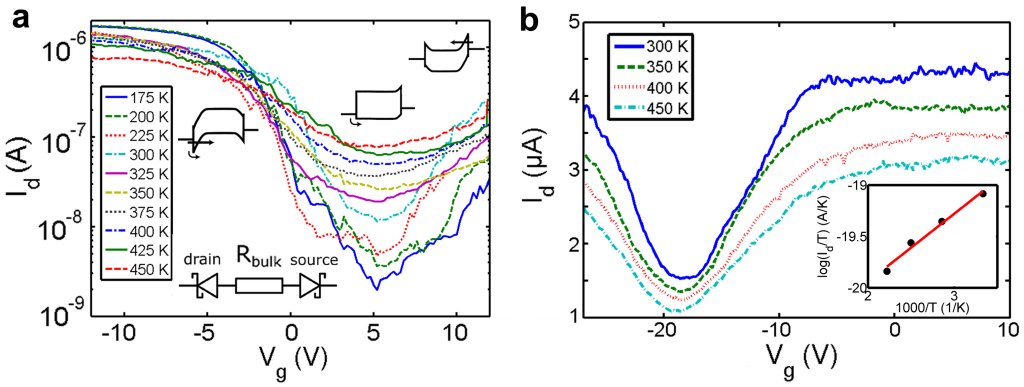

Figure 6.5: *Transfer characteristics of Pd contacted CNTs at different temperatures with $V_d = 100$ mV. a) Semiconducting CNT. The upper insets show schematic band diagrams at three different gate voltages. The lower inset shows the equivalent circuit of the CNTFET. b) Small band gap semiconducting CNT. The inset displays I_d at $V_g = -18$ V for different temperatures in an Arrhenius plot.*

and a poor on/off ratio has a temperature dependence which is dominated by scattering in the bulk of the CNT at all gate voltages due to the low SBs (figure 6.5b). Therefore, if the series resistance dominates transport it is not possible to reliably extract any SB height from the measurements. This implies that the SB height can only be extracted at some gate voltages and the CNTs should be short to avoid that bulk scattering dominates.

If the series resistance is disregarded and image force lowering is the only barrier lowering mechanism, the net thermionic emission current through a metal-CNT-metal structure with contacts with equal work functions and a positive voltage V_d applied to the drain is

$$I_{TE} = I_{se} + I_{dh} - I_{sh} - I_{de} \tag{6.6}$$

where

$$I_{se} = A_s A_e^* T e^{-q(\Phi_{SBe} - \Delta\Phi_{SBe})/k_B T} \tag{6.7}$$

is the electron current from the source,

$$I_{dh} = A_d A_h^* T e^{-q(\Phi_{SBh} - \Delta\Phi_{SBh})/k_B T} \tag{6.8}$$

the hole current from the drain,

$$I_{sh} = A_s A_h^* T e^{-q(\Phi_{SBh} - \Delta\Phi_{SBh} + V_d)/k_B T} \tag{6.9}$$

the hole current from the source and

$$I_{de} = A_d A_e^* T e^{-q(\Phi_{SBe} - \Delta\Phi_{SBe} + V_d)/k_B T} \tag{6.10}$$

the electron current from the drain, A_s (A_d) the source (drain) contact area, A_e^* (A_h^*) the effective Richardson's constant for electrons (holes) and $\Delta\Phi_{SBe}$ ($\Delta\Phi_{SBh}$) the image force lowering for electrons (holes) (figure 6.6) [192]. That the current in the hole branch at negative gate voltages is much higher than that in the electron branch at positive gate voltages indicate that the barrier for holes (Φ_{SBh}) is smaller than that for electrons (Φ_{SBe}). Due to the exponential dependence of the thermionic emission current on barrier height, a device with a difference in barrier heights of only $\Phi_{SBe} - \Phi_{SBh} =$ 50 mV at a bias of $V_d = 100$ mV gives a ratio between forward and reverse hole currents of $I_{dh}/I_{sh} = 7$ and between forward hole and electron currents of $I_{dh}/I_{se} = 55$ at room temperature for equal source and drain contact areas and hole and electron Richardson's constants. Thus, the hole barrier at the drain dominates transport and the electron currents and the reverse hole current can be disregarded in eq. 6.6 and the net thermionic emission current simplified to

$$I_{TE} \approx I_{dh} = A_d A_h^* T e^{-q(\Phi_{SBh} - \Delta\Phi_{SBh})/k_B T}. \tag{6.11}$$

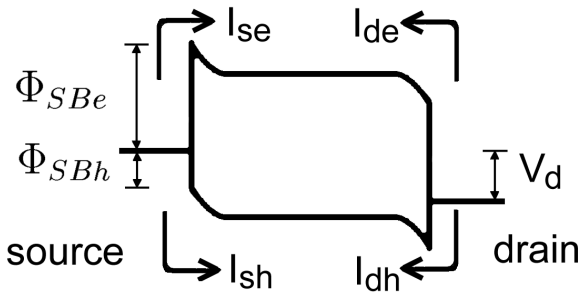

Figure 6.6: *Schematic band diagram of a CNT contacted by two identical metal electrodes at a positive bias of V_d applied to the drain. The SB for electrons (Φ_{SBe}) is higher than that for holes (Φ_{SBh}). I_{se} is the thermionic emission current of electrons from the source, I_{de} the electron current from the drain, I_{sh} the hole current from the source and I_{dh} the hole current from the drain.*

To extract SB heights, the data from the transfer characteristics are plotted in an Arrhenius plot from which activation energies are extracted at all gate voltages by a linear fit to the highest temperatures (figure 6.7a). The

activation energy plotted as a function of gate voltage shows a maximum of $E_{a,max}$, which corresponds to the SB height for holes, at a gate gate voltage of $V_{g,max}$ with decreasing activation energy at high negative or positive gate voltages indicative of increased tunneling or barrier lowering (inset in figure 6.7a). To accurately estimate Φ_{SBh} by $E_{a,max}$, any influence of barrier lowering mechanisms should be small and there should be no additional barrier induced by the gate voltage. The maximum activation energy does not decrease considerably with increasing V_d up to a few hundred mV but at higher biases it is reduced considerably (figure 6.7b). The lowering of the activation energy at high V_d could be due to image force lowering, potential drops over an interfacial layer or tunneling but the relative impact of each or these mechanisms is difficult to elucidate. However, it can be concluded that the small bias of $V_d = 100$ mV does not result in considerable barrier lowering and $\Delta\Phi_{SBh}$ in eq. 6.11 is thus negligible.

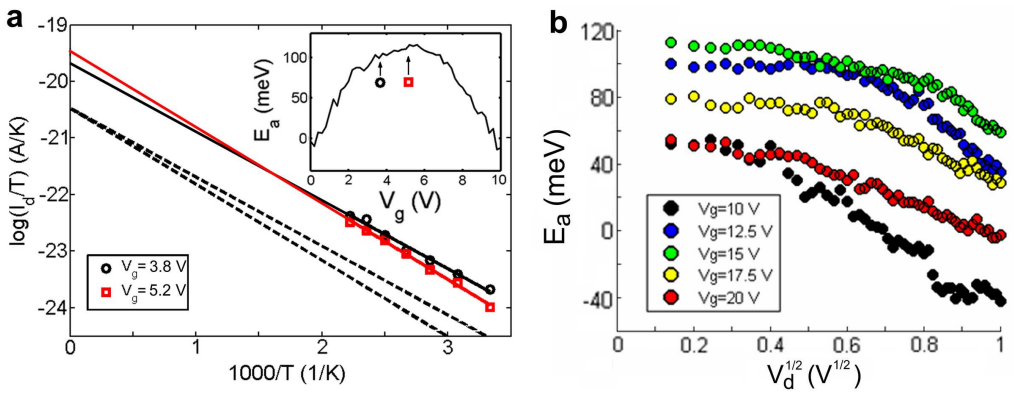

Figure 6.7: *a) Arrhenius plot of the data in figure 6.5a (symbols) at two different gate voltages and linear fits (solid lines). The two dashed lines display the expected result for a theoretical thermionic emission current described by eq. 6.11 with an activation energy corresponding to the two different gate voltages used. The theoretical lines have been offset vertically for clarity. The inset displays the activation energy vs gate voltage with the two gate voltages used in the Arrhenius plot indicated. The square symbol indicates the maximum activation energy $E_{a,max}$ at the gate voltage $V_{g,max}$. b) Activation energy as a function of $V_d^{1/2}$ extracted from IV_d characteristics at a few different gate voltages. The gate voltages can not be directly compared to those in the inset in a) due to threshold voltage shifts.*

Changing the gate voltage from that which gives the maximum activation energy gives a lower slope in the Arrhenius plot (figure 6.7a). If the lower slope is a result of only decreased thermionic emission there should be a ver-

tical shift of the curves since the Richardson's constants and contact areas are unchanged. However, the intersection with the y-axis is not constant which is expected if thermionic emission is the only mechanism contributing to the current. Therefore we conclude that barrier lowering and/or tunneling occurs at gate voltages larger or smaller than $V_{g,max}$. This means that $V_{g,max}$ corresponds to the band bending situation close to that shown in figure 6.6 where thermionic emission from the drain dominates and thus $E_{a,max}$ is a good estimate of the SB height.

The SB heights measured for several CNTs decrease with diameter (figure 6.8a). Measurements on CNTFETs with multiple contacts and CNT segments of different lengths (400 nm to 10 μm) give similar SB heights indicating that scattering in the bulk of the CNTs can be disregarded and that the diameter of the CNTs is the main factor determining the SB height. Data points from Chen et al. [167] who calculated SB heights from the on currents of CNTFETs and Léonard et al. who calculated SB height as a function of CNT diameter using an analytical model of the electrostatics considering the depletion width to be limited to the CNT diameter [164] are also included in figure 6.8a. The solid line shows the expected hole SB height for the Shottky-Mott limit without influence of interface states given by

$$\Phi_{SBh} = \phi_{CNT} - \phi_m + \frac{E_g}{2} \tag{6.12}$$

where $\phi_{CNT} = 5.0$ eV is the CNT work function, $E_g = 0.8/d$ eV the CNT band gap and $\phi_m = 5.12$ eV the Pd work function. All three results show a decreasing SB height with increasing diameter, however there is a large discrepancy in the SB heights. The SBs calculated by Léonard et al. are lower than what we obtained, a result that can be explained by the large difference in the work functions used in their calculations ($\phi_m - \phi_{CNT} =$ 0.4 eV). The SBs measured by Chen et al. also show lower barriers and in addition the SBs decrease faster with diameter than expected from the Schottky-Mott description. A fit using eq. 6.12 to their data gives a work function difference of 0.5 eV and a $E_g = \alpha/d$ relation with $\alpha = 0.6$ eV $\cdot$ nm. A major difference between the two experiments is that our devices were measured in vacuum while those of Chen et al. were measured in air. Figure 6.9 displays the transformation of the transfer characteristic as a Pd contacted CNTFET is heated in vacuum. Initially, the device is p-type with a negligible electron branch but when heated to 450 K the characteristic becomes ambipolar which is preserved as it is cooled down. Exposure to N_2

at atmospheric pressure changes the characteristic to slightly more p-type and as the environment is changed to air the characteristic reverts almost fully to the initial p-type state. Since the shift of the threshold voltage is negligible it can be concluded that the transformation is not an effect of changed doping but that instead the work function of Pd decreases as adsorbed water and oxygen molecules are removed during heating [62]. That Pd has a lower work function compared to other experiments performed in air is most likely the reason that the diameter needed to obtain a zero SB is larger in our experiments than others [167, 181]. For our data, the large uncertainty in the CNT diameters is because they were measured using AFM and that the surface of the substrate was rough, probably due to resist residues left after fabrication (figure 6.8c). Using TEM would make the diameter determination much more accurate but combining it with electrical measurements requires complex sample fabrication.

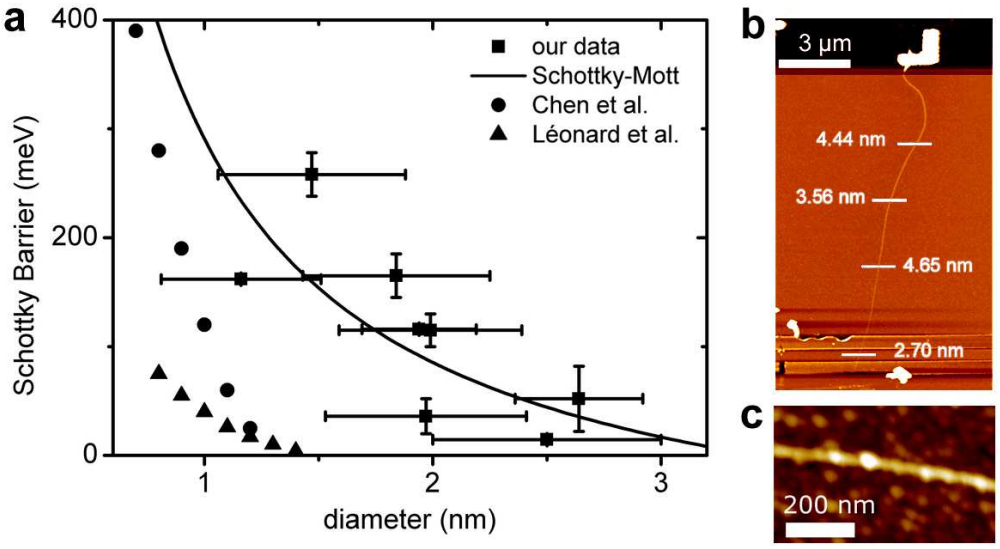

Figure 6.8: *a) SB height for holes as a function of CNT diameter for Pd contacted CNTs for our measurements, experimental data from Chen et al. [167] and theoretical calculations from Léonard et al. [164]. Note that the data point for the largest diameter CNT included in paper VI has been omitted since it corresponds to a measurement on a bundle. b) AFM image of the largest diameter CNT included in paper VI which shows a variation of the CNT height relative to the surface, indicated by four horizontal lines, a strong indication that it actually is a bundle of several CNTs. c) AFM image of a CNT with possible resist residues on the surface.*

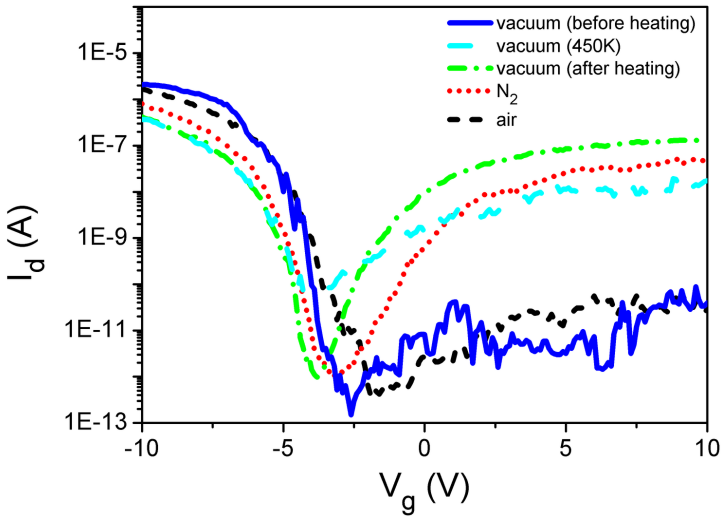

Figure 6.9: *Transfer characteristics of a Pd contacted CNT with $V_d = 100$ mV at different stages of heating in vacuum and after exposure to N_2 and air.*

However, since the uncertainties in the work functions of both CNTs and Pd are large and the measurement of the diameter is inaccurate, it is hard to determine whether dipole formation at the interface has any effect on the SB heights i.e. if we have any Fermi level pinning in CNT-metal contacts. However, the results clearly show that the SB decreases with increasing CNT diameter, an effect which is attributed to the decrease in band gap. In addition, the measurements indicate that a CNT diameter larger than 2 nm is needed to obtain a SB height close to zero for a Pd contacted CNT in vacuum.

6.6 Schottky barrier heights for different metal contacts to CNTs

To investigate the effect of Fermi level pinning and at the same time alleviate the problem of uncertainties in the measurements of the CNTs diameters and their work functions, samples with contacts of different metals on the same CNT have been fabricated (figure 6.10a). If each metal would be deposited on different CNTs, it would be difficult to separate the impact of any variation in CNT diameter from that of the different metal work functions on the SB height. If there is no effect of Fermi level pinning, the change in SB height using different metals should be equal to the corresponding difference in metal work functions ($\gamma = 1$ in eq. 6.2) but if interface states have an impact, there should only be a small variation of the SB height with work function ($\gamma \approx 0$ in eq. 6.2). The results presented in this chapter are preliminary and should be viewed with some caution since there are still some unresolved issues that have to be clarified to draw definite conclusions about the influence of Fermi level pinning in CNT-metal contacts.

The different metals that have been tested are Pd, Au, Cr, Ti, Al and Sc since they cover a large span of work functions (3.5-5.12 eV) and have good adhesion to the SiO_2 substrates. Since the off state current of a single CNT is usually low, source and drain electrodes with multiple interdigitated fingers have been used. This corresponds to having several segments of the same CNT connected in parallel which increases the current. Devices with Al and Sc electrodes often exhibited unstable characteristics with a high resistance initially which was lowered after a current of 10 μA was passed through them. However, the low resistance state lasts a few hours in vacuum but only a few minutes in air, an effect which could be due to oxidation of the metal. Due to this unstable behaviour, it was difficult to perform temperature dependent measurements to obtain reliable values of the SB heights for Al and Sc contacted CNTs. The transfer characteristics measured for Pd, Ti and Cr electrodes on the same CNT (figure 6.10b) show that the current in the p-branch increases while the n-branch and the off state decrease with increasing work function. This change implies that the Fermi level of the metal moves closer to the top of the valence band as the work function is increased and thus holes are more easily injected into the CNT (figure 6.3b). The higher off state current for low work function metals is because both holes and electrons can easily be injected into the CNTs using contacts with metal work functions that give a Fermi level close to the middle of the band gap. If different metals are used as source and

drain electrodes, a device acts as a Schottky diode with a large difference in current between forward and reverse biases due to the dissimilar SB heights (inset in figure 6.10b).

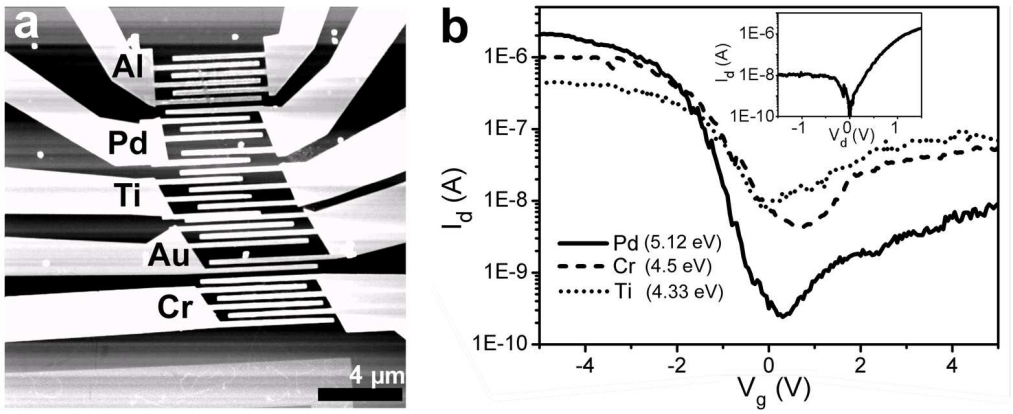

Figure 6.10: *a) AFM image of interdigitated electrodes of five different metals on a CNT. b) Transfer characteristic in vacuum using Pd, Ti or Cr electrodes (work functions in parentheses) on the same CNT. The inset shows the IV_d characteristic using one Pd and one Ti contact on another CNT.*

To avoid the hysteresis and threshold voltage shifts that are commonly observed when measuring transfer characteristics at different temperatures, the output characteristic was measured with the back gate at a floating potential (figure 6.11a). Since the contacts act as two Schottky diodes connected back-to-back where the resistance of the forward biased diode can be neglected, the current at both polarities can be described by eq. 6.4 with a negative V_d. The ideality factor, extracted from the slope of a linear fit to $log(I_d/(1 - exp(-qV_d/k_BT))$ vs V_d, is n=1.1 and varies only a little within the temperature range used (figure 6.11b). Such a low ideality factor implies that thermionic emission dominates the transport and justifies that eq. 6.4 is used to describe the data. Activation energies are extracted from Arrhenius plots of the data (figure 6.11c) and plotted as a function of $V_d^{1/2}$ (figure 6.11d). A linear fit is used to extract the intersection at $V_d = 0$ V which corresponds to an effective SB height at zero bias. The actual SB height could be slightly higher due to barrier lowering caused by any built in voltage. The $V_d^{1/2}$ dependence indicates that the barrier lowering is due to the potential drop over an interfacial layer at the contact [151].

The SB heights for different metal contacts on a CNT are all within 100-300 meV but reveal no clear trend as a function of metal work function

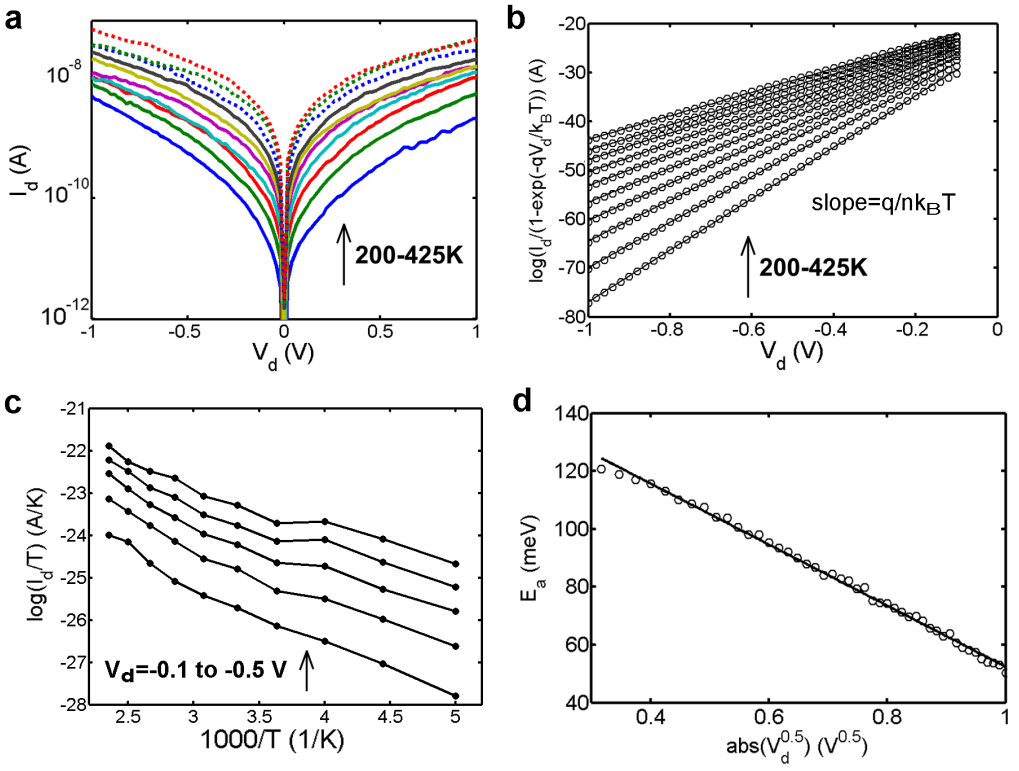

Figure 6.11: *a) IV_d characteristics of a Ti contacted CNT at 200-425 K (25 K increments) without voltage applied to the gate. b) Plot of the data in a) (circles) with linear fits (lines) for the extraction of the ideality factor at different temperatures. c) Arrhenius plot of the data in a) for V_d =0 to -0.5 V (0.1 V steps). d) Activation energy as a function of $V_d^{1/2}$. An effective Schottky barrier is extracted at the intersection of a linear fit with the y-axis.*

(figure 6.12a). For a device with four different metals, the SB height extracted for the Au contact is higher than those for the Ti and Cr contacts which have lower work functions. The data indicate however that the SB heights do not have a one-to-one correspondence with the metal work function which implies that interface states or chemical bond polarisation could influence the SBs. This result agrees well with Perello et al. who also used temperature dependent IV_d measurements and extracted equal SB heights for Cr, Mo and Ni contacts on a single CNT [193].

The work functions used in figure 6.12a are from measurements on a clean surface in vacuum, however the work functions of metals are very sensitive to contaminants, e.g. the work function of Au can be reduced by

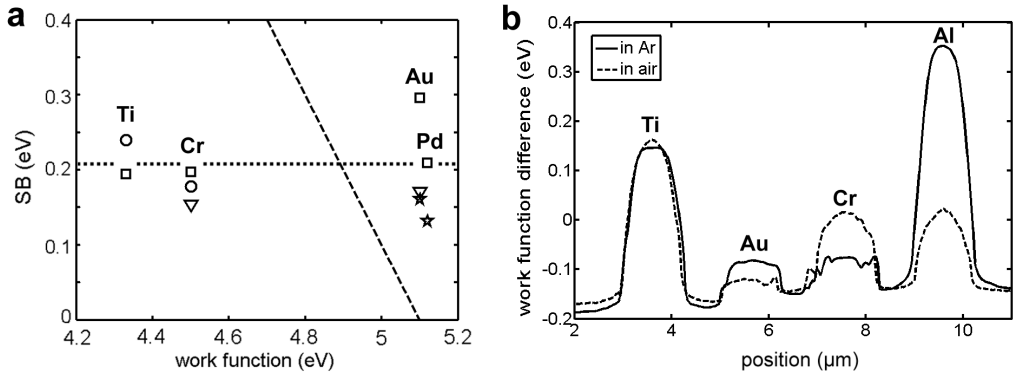

Figure 6.12: *a) SB height as a function of metal work function [194] for three CNTs contacted by up to four different metals. The dashed line shows the expected hole SB for CNT-metal contacts without pinning and the dotted line the hole SB for a Fermi level pinned to the middle of the band gap for a CNT with a diameter of 2 nm. The IV_d data and Arrhenius plots for the devices is presented in appendix B. b) Work function difference between a TiN coated tip and different metals measured using KPFM in air and in Ar. The metals are all deposited on a Pd surface.*

up to 0.6 eV when exposed to air [195]. To measure their work function, the electrodes have been studied using Kelvin probe force microscopy (KPFM) [196]. KPFM is a technique that uses an AFM setup to measure the local work function difference between a conducting tip and a surface. As two materials are electrically connected, their Fermi levels equilibrate and a contact potential difference equal to the difference in work functions develops. In KPFM, the surface topography is first measured in semi-contact mode and then the cantilever is lifted up a few 10s of nm and during a second pass, an AC voltage is applied to the tip to oscillate the cantilever at its resonance frequency while the surface is grounded. A DC bias is applied to the tip to nullify the attractive force that arises between the tip and the surface due to the work function difference, thereby minimising the amplitude of the cantilever. This DC bias gives a measure of the local work function of the surface relative to the work function of the metal coated tip. To study the effect of adsorbents, KPFM has been performed on electrodes of different metals deposited on a Pd surface both in air and in Ar after heating in vacuum (figure 6.12b). Since the work function of the TiN coated tip is unknown, it is only possible to deduce differences between the work functions of the metals. The work function differences are lower than those measured in vacuum [194] but follow the same trend

($\phi_{Pd} > \phi_{Au} > \phi_{Cr} > \phi_{Ti}$) with the exception of Al in Ar. It is evident that the environment has a large impact, with up to 330 mV difference of the work function of Al in air and in Ar. However, since the work functions in vacuum may differ from those measured in Ar, more efforts are needed to clarify the effect of metal work function on SB heights and the influence of Fermi level pinning.

6.7 Conclusions

The measurements of the SB heights as a function of CNT diameter confirm that large CNTs have to be used to obtain CNTFETs with negligible SBs. However, even though large diameter CNTs have the additional benefit of a high mobility [67] their small band gaps lead to high off state currents resulting in a trade-off between switching speed and leakage current. The magnitude of the SB heights measured on Pd contacted CNTs are in agreement with what is expected without Fermi level pinning but since the reported values of the work functions of both Pd and CNTs vary significantly, any impact of interface states can not be completely ruled out.

From an engineering perspective, it is possible to obtain good contacts to CNTs by choosing a metal with high or low work function for p or n type CNTFETs respectively and by using CNTs with sufficiently large diameter. However, there is still a lack of understanding of the details of the SB formation and the influence of interface dipoles. Theoretical modeling gives a wealth of different results predicting either no influence of interface states [164, 165], a high sensitivity to the microscopic bonding configuration and crystal orientation [176, 177] and even that a semiconducting CNT underneath a contact becomes metallic-like [166, 173].

The poor understanding of the most important factors that affect SB formation in metal-CNT contacts stems from the difficulty in using many of the techniques available for bulk materials to perform measurements on SBs in nanoscale contacts. The temperature dependent electrical measurement technique presented here is presently the only method to obtain quantitative SB heights without the need for theoretical modeling but as capacitive [186] and optical [189] measurement techniques continue to improve, a deeper understanding of the physics of nanoscale contacts can hopefully be obtained.

Chapter 7

Outlook

This final chapter is dedicated to a discussion on the challenges that Si MOSFETs face as they are scaled down and why CNTs is a viable option as a replacement for Si. Si has been the dominant material in MOSFETs for logic circuits since their invention in the 1960's [197]. Even though Si has a poor mobility compared to other semiconductors such as Ge, GaAs, InAs and InSb, its low cost and good oxide interface has enabled it to retain its dominant position within the semiconductor industry. The steady increase in computing power has mainly been possible by reducing the gate length which lowers the gate delay time leading to higher operating frequencies. However, the gate electrode has to maintain good electrostatic control of the potential in the channel as the gate length is reduced which is achieved through a reduction of the thickness or an increase of the dielectric constant of the gate dielectric. To ensure good control, the gate dielectric thickness has now been reduced below 1 nm resulting in large leakage currents. To alleviate the problem of poor gate control, new device designs have been developed with multiple gates or thin Si channels that improve the control of the channel compared to a bulk MOSFETs [198]. Using nanowires can further improve the electrostatics and enable short gate lengths since gate electrodes that wrap around the wires can be fabricated [199].

Another approach to improve the performance of MOSFETs is to replace Si with a material with a higher mobility which results in higher on currents and therefore a reduced gate delay. Thus, the same performance can be achieved at a longer gate length which relaxes the requirement for aggressive scaling of the gate dielectric thickness. These two approaches for transistor improvement can be combined by making devices with reduced

dimensionality for improved electrostatic control using materials with a high mobility, an approach demonstrated in nanowires made from III/V materials, CNTFETs or graphene FETs. However, the mobility of InAs nanowires is substantially lowered as the diameter is reduced due to increased surface scattering [69]. Therefore, there is a trade-off between good electrostatic control and high mobility for these devices.

In contrast to a nanowire, all the carbon atoms in a CNT are situated on its surface and there are no dangling bonds present, resulting in low surface scattering. Most research on CNTFETs is presently done in academic institutions, but the semiconductor industry shows an increasing interest in using CNTs for large scale integrated circuits. The most important challenges that need to be solved to make CNTFETs a viable replacement for Si have been identified by the ITRS and the time needed to solve them has been estimated (figure 7.1). It should however be noted that academic research has already presented solutions to several of the identified issues such as reliable ohmic contacts, integration of high-k dielectrics and control of the number of walls in the CNTs.

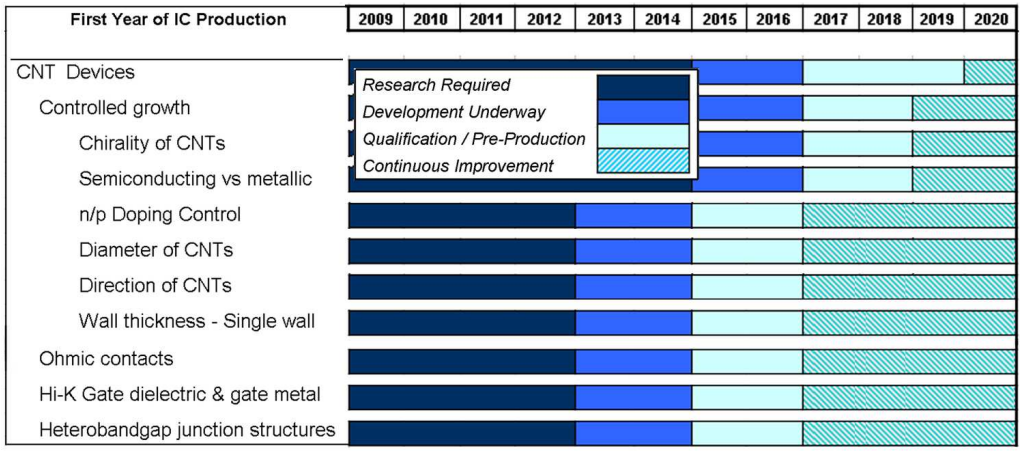

Figure 7.1: *Challenges for the development of CNTFETs for integrated circuits identified by ITRS [3].*

The results presented in this thesis address two of the challenges, directional control of CNTs during growth which is achieved using an electric field and the formation of an ohmic contact to semiconducting CNTs which is studied through a measurement of the SB heights for CNTs with different diameter. The major obstacle for a large scale integration of CNTFETs is

the lack of control of their structure. To separate or controllably grow either semiconducting or metallic CNTs their diameters have to be controlled with a precision better than 0.7 Å for CNTs with diameters around 1.5 nm and CNTFETs with multiple CNTs as the channel have to contain less than 0.05% metallic CNTs to give the on/off ratio of 3000 required for logic applications [200]. This stringent requirement has so far limited the performance of logic transistors with multiple CNTs in the channel but results on selective destruction of metallic CNTs [71] or the use of semiconducting CNTs separated by centrifugation [201] illustrate that there are methods to alleviate this problem.

Since some of the most fundamental problems for large scale fabrication of CNTFETs are still unresolved, the attention of the semiconductor device community has shifted towards graphene as a possible replacement for Si [202]. Like CNTs, graphene has high mobility and allows for good electrostatics since it only consists of a single atomic layer. In contrast to CNTs there is hope that graphene FETs will have less variability in their characteristics and more simple integration into large scale circuits due to the possibility of patterning desired structures. However, graphene is a semimetal and thus the on/off ratios of graphene FETs are too low to be used for logic applications. A band gap can be induced in a graphene by spatial confinement of the electron wavefunctions by lithographically [203] or chemically [204] creating narrow ribbons or by fabricating a dense array of holes in the sheet [205]. However, the widths of the produced nanoribbons are still too large to induce a band gap comparable to that of CNTs and any irregularity in the edges has a large impact on device performance [206]. Other possibilities for band gap engineering are to use a high electric field applied perpendicular to a double layer graphene sheet [207] or to chemically oxidise [208] or hydrogenate [209] graphene. Therefore, even though graphene FETs solves some of the major challenges present for CNTFETs, new problems arise that may be equally difficult to overcome.

The tough requirements on a small variability in device characteristics, low cost of production and high yield set by the semiconductor industry makes the introduction of exotic materials like CNTs in mass production of logic circuits difficult. Therefore, it is expected that it will still take many years before the processor in your desktop computer is filled with CNTs. Meanwhile, there are still many exciting technological challenges that have to be addressed obtain even better CNTFETs as well as more fundamental questions to be answered concerning the electronic transport in CNTs.

Chapter 8

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Appendix A

Detailed sample fabrication

This appendix describes the most important process steps in the sample fabrication. The substrates used are 2" highly doped n++ Si wafers with a 100 nm, 400 nm or 1 μm thick oxide.

Marks and catalyst

This EBL process is mainly used to make alignment marks, electrodes for electric field directed growth but also for contacts to CNTs with sizes down to 400 nm.

1. Spin LOR3A at 3000 rpm for a thickness of 280 nm. Bake 3 min at 180°C.
2. Spin UV5-0.6 at 4000 rpm for a thickness of 650 nm. Bake 1 min at 130°C.
3. Expose marks and electrodes using EBL with a current of 10 nA and a dose of 45 $\mu C/cm^2$.
4. Postbake for 1.5 min at 130°C.
5. Develop in MF24A for 35 s and ash in O_2 plasma at 50 W for 15 s.
6. Deposit 5 nm Ti / 100 nm Mo using e-gun evaporation.

7. Lift-off in Shipley 1165 remover heated to 60°. Rinse in IPA and water, blow dry.

8. Pattern catalyst areas using the same recipe as for the electrodes and deposit 5 nm Al_2O_3 / 0.5 nm Fe using e-gun evaporation.

Electric field aligned growth of CNTs with substrate deformations

1. Place sample on a quartz holder with clamps connected to a voltage supply. Sample should be positioned ∼30 cm from the opening of the furnace. Evacuate quartz tube down to 1 mbar. Fill chamber with Ar up to atmospheric pressure.

2. Heat the furnace to 970°C in a flow of 500 sccm[1] Ar and 100 sccm H_2.

3. Exchange the Ar to CH_4 with a flow rate of 1000 sccm. Move the quartz tube so that the sample is positioned ∼8 cm into the furnace. Lower the temperature to $900°C$.

4. After 3 min of growth, switch on the voltage supply to apply a field of about 1 V/µm over the gaps. Grow for 10-20 min.

5. Switch off the furnace and change CH_4 to Ar while cooling the system.

Contacts to CNTs

This EBL process is used for features with sizes smaller than 400 nm.

1. Locate CNTs using SEM and design electrodes according to their positions.

2. Spin copolymer MMA(8.5)MAA EL4 at 3000 rpm for a thickness of 80 nm. Bake at 170°C for 5 min.

[1] cubic centimeter per minute at standard temperature and pressure.

3. Spin ZEP520 (1:1 Anisole) at 3000 rpm for a thickness of 120 nm. Bake at 170°C for 5 min.
4. Expose at 1 nA with a dose of 370 $\mu C/cm^2$.
5. Develop in hexylacetate for 1 min, rinse in IPA, develop in MIBK/IPA (1:2) for 2 min, rinse in water and blow dry.
6. Deposit 0.5 nm Ti / 30 nm Pd using e-gun evaporation.
7. Lift-off in Shipley 1165 remover.

Pads for electrical probing

This photolithography process is used for large features that do not require good alignment to any previous pattern.

1. Spin LOR3A at 3000 rpm for a thickness of 380 nm. Bake at 180°C for 3 min.
2. Spin S1813 at 4000 rpm for a thickness of 1.3 μm. Bake at 110°C for 2 min.
3. Expose with an intensity of 1.5 mW/cm^2 for 50 s through a photomask.
4. Develop in MF319 for 35 s.
5. Oxygen plasma at 50 W for 15 s.
6. Deposit 5 nm Ti / 120 nm Au.
7. Lift-off in Shipley 1165 remover.

Atomic layer deposition and etching of the dielectric

1. Heat the substrate to 150°C. The chamber pressure during the reaction is 10 mbar.

2. Pulse tri methyl aluminum into the chamber for 0.1 s.
3. Flow N_2 for 4 s to purge the chamber.
4. Pulse H_2O for 0.1 s.
5. Flow N_2 for 4 s to purge the chamber. A monolayer of Al_2O_3has now been deposited. Repeat from step 2 until the desired film thickness is reached.
6. Pattern resist using the same recipe as for the marks and catalyst but without the LOR underlayer.
7. Etch Al_2O_3 at a rate of 2 nm/min using a 30 mA Ar ion beam with an energy of 500 V.
8. Remove the resist in Shipley 1165.

Dielectrophoresis of gate CNTs

1. Bond the pads to a custom made chipholder.
2. Deposit a small amount of CNTs dispersed in SDS solution (2 weight %) on the chip using a pipette.
3. Apply an AC voltage of 2-4V/μm and a frequency 20 MHz across the gaps for 5-30 s.
4. Rinse off remaining solution using water and blow dry.

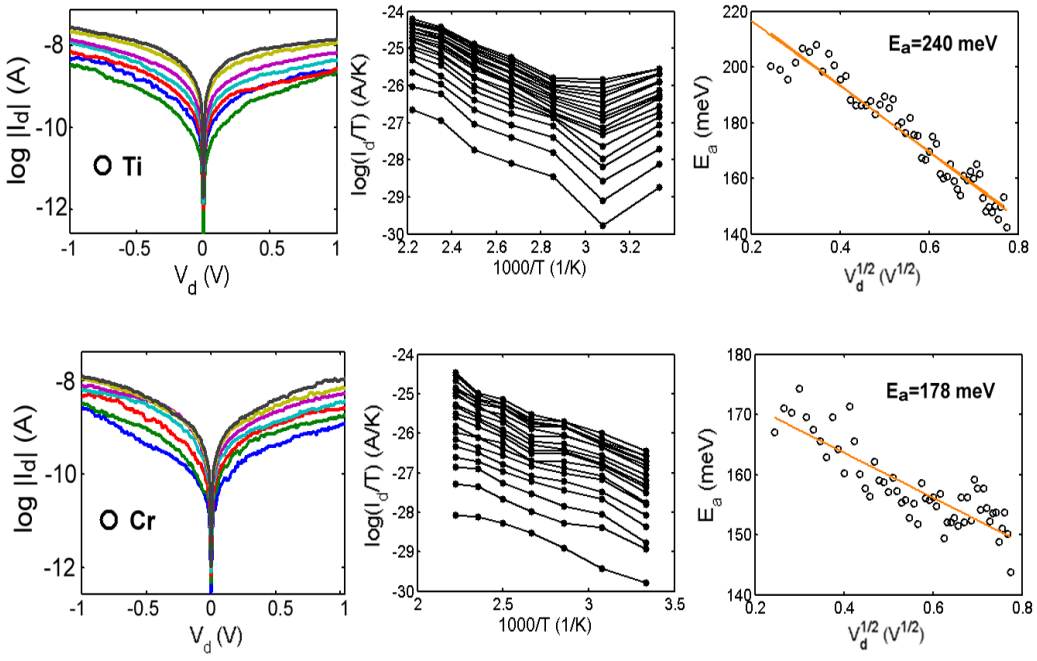
Deposition and etching of Si_3N_4

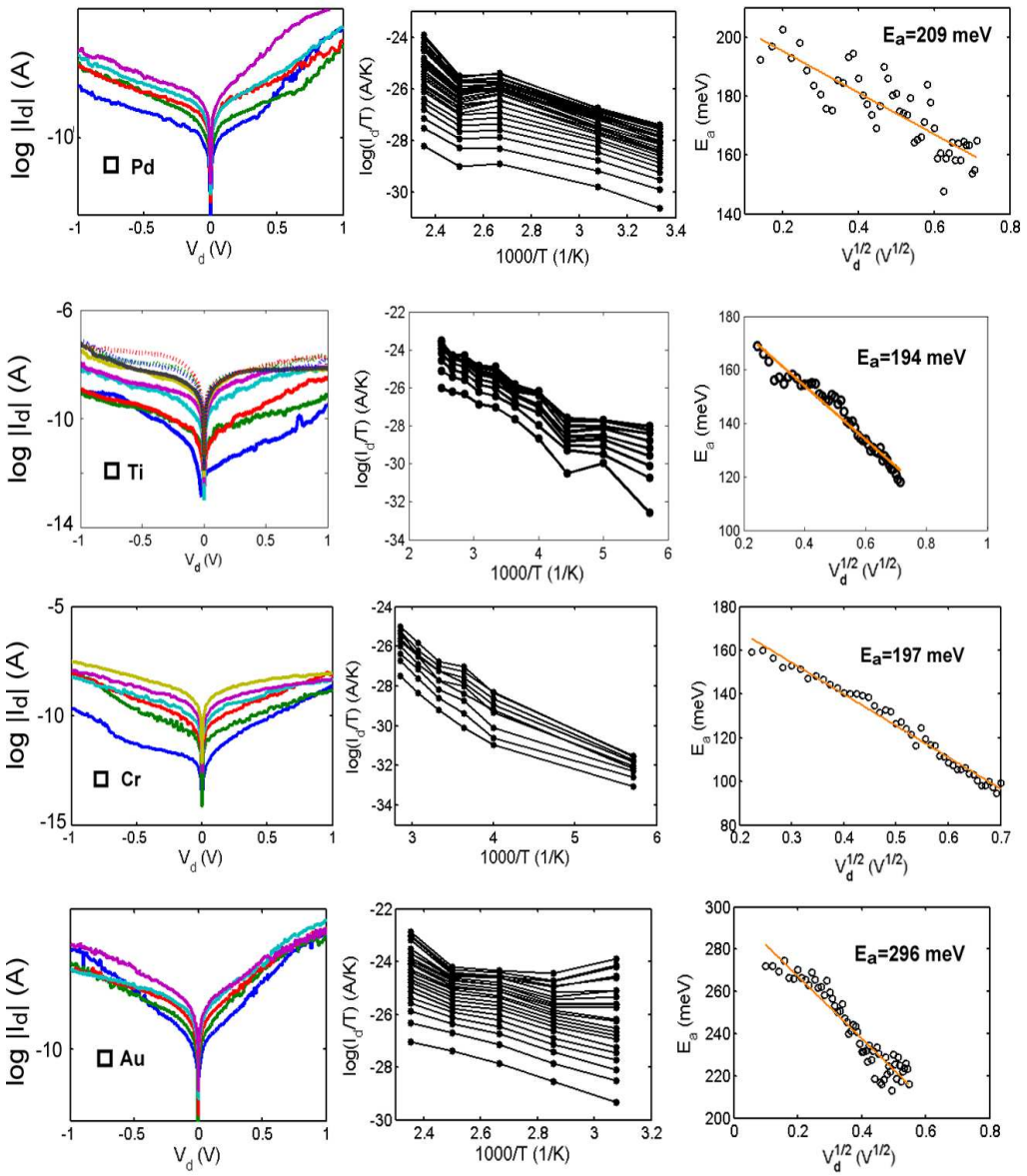
1. Deposit Si_3N_4 at 300°C at a rate of 0.16 nm/s using PECVD with 2000 sccm SiH_4 and 40 sccm NH_3 at a power of 20 W and a pressure of 800 mTorr.
2. Pattern resist using the same recipe as for the marks and catalyst but without the LOR underlayer.
3. Etch Si_3N_4 at a rate of 1 nm/s using RIE with 10 sccm Ar and sccm CF_4 at a power of 50W and a pressure of 20 mTorr.
4. Remove the resist in Shipley 1165.

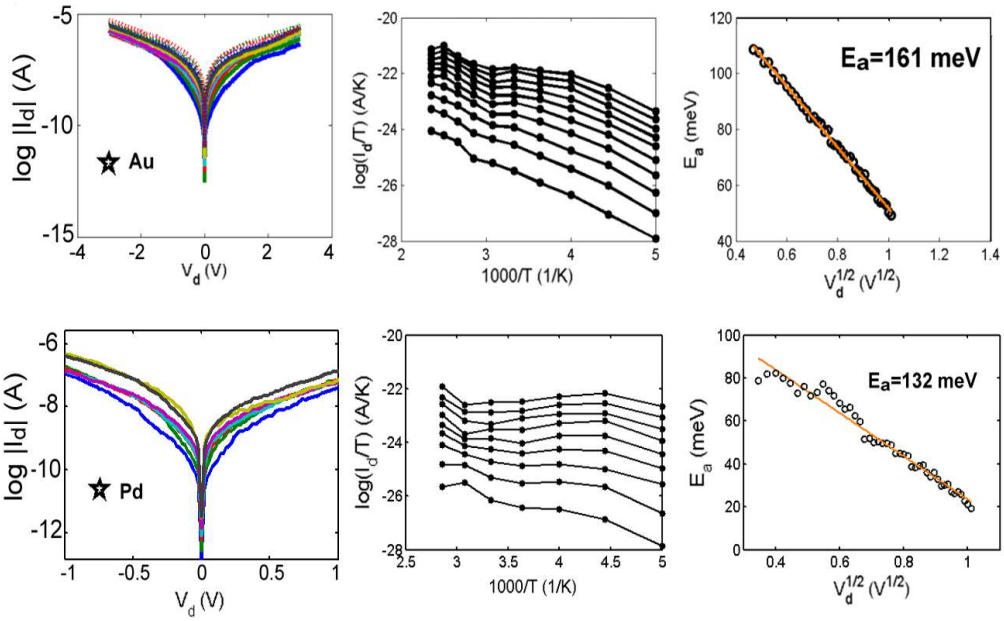
Appendix B

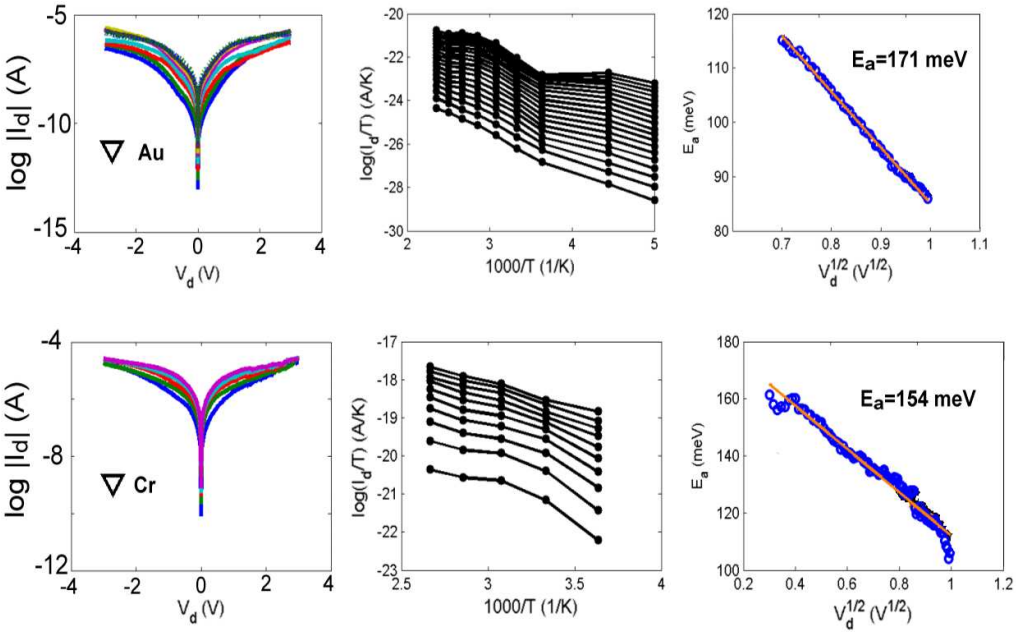
Data for different metal-CNT contacts

IV_d characteristics at 175-450 K, the corresponding Arrhenius plots and E_a as a function of $\sqrt{V_d}$ for the four devices in figure 6.12. The IV_d have been measured in vacuum with floating gate voltage.




log |I_d| (A)
Pd
V_d (V)
log(I_d/T) (A/K)
1000/T (1/K)
E_a=209 meV
E_a (meV)
V_d^1/2 (V^1/2)
log |I_d| (A)
Ti
V_d (V)
log(I_d/T) (A/K)
1000/T (1/K)
E_a=194 meV
E_a (meV)
V_d^1/2 (V^1/2)
log |I_d| (A)
Cr
V_d (V)
log(I_d/T) (A/K)
1000/T (1/K)
E_a=197 meV
E_a (meV)
V_d^1/2 (V^1/2)
log |I_d| (A)
Au
V_d (V)
log(I_d/T) (A/K)
1000/T (1/K)
E_a=296 meV
E_a (meV)
V_d^1/2 (V^1/2)


log |Id| (A)
Au
Vd (V)
log(Id/T) (A/K)
1000/T (1/K)
Ea (meV)
Ea=161 meV
Vd1/2 (V1/2)
log |Id| (A)
Pd
Vd (V)
log(Id/T) (A/K)
1000/T (1/K)
Ea (meV)
Ea=132 meV
Vd1/2 (V1/2)


log |Id| (A)
Au
Vd (V)
log(Id/T) (A/K)
1000/T (1/K)
Ea (meV)
Ea=171 meV
Vd1/2 (V1/2)
log |Id| (A)
Cr
Vd (V)
log(Id/T) (A/K)
1000/T (1/K)
Ea (meV)
Ea=154 meV
Vd1/2 (V1/2)

Paper I

Electric field aligned growth of single-walled carbon nanotubes

*Current Applied Physics, **4**, 595-598, (2004)*

Paper II

Marangoni effect in SiO_2 during field-directed chemical vapor deposition growth of carbon nanotubes

Physical Review B, ***73****, 205413, (2006)*

Paper III

Field emission induced deformations in SiO_2
during CVD growth of carbon nanotubes

*Physica Status Solidi (b), **243**, (13), 3524-3527, (2006)*

Paper IV

Fabrication of Crossed Junctions of Semiconducting and Metallic Carbon Nanotubes: A CNT-Gated CNT-FET

Journal of Nanoscience and Nanotechnology, ***6****, (5), 1325-1330, (2006)*

Paper V

A carbon nanotube gated carbon nanotube transistor with 5 ps gate delay

Nanotechnology, ***19****, 325201, (2008)*

Paper VI

The dependence of the Schottky barrier height on carbon nanotube diameter for Pd–carbon nanotube contacts

Nanotechnology ***20****, 175204, (2009)*